RELIABILITY REPORT

FOR

MAX19985AETX+

PLASTIC ENCAPSULATED DEVICES

November 18, 2008

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX19985AETX+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX19985A high-linearity, dual-channel, downconversion mixer is designed to provide approximately 8.7dB gain, +25.5dBm of IIP3, and 9.0dB of noise figure for 700MHz to 1000MHz diversity receiver applications. With an optimized LO frequency range of 900MHz to 1300MHz, this mixer is ideal for high-side LO injection architectures in the cellular and new 700MHz bands. Low-side LO injection is supported by the MAX19985, which is pin-pin and functionally compatible with the MAX19985A. In addition to offering excellent linearity and noise performance, the MAX19985A also yields a high level of component integration. This device includes two double-balanced passive mixer cores, two LO buffers, a dual-input LO selectable switch, and a pair of differential IF output amplifiers. On-chip baluns are also integrated to allow for single-ended RF and LO inputs. The MAX19985A requires a nominal LO drive of 0dBm and a typical supply current of 330mA at VCC = +5.0V or 280mA at VCC = +3.3V. The MAX19985/MAX19985A are pin compatible with the MAX19995/MAX19995A series of 1700MHz to 2200MHz mixers and pin similar with the MAX19997A/MAX19999 series of 1850MHz to 3800MHz mixers, making this entire family of downconverters ideal for applications where a common PCB layout is used across multiple frequency bands. The MAX19985A is available in a 6mm x 6mm, 36-pin thin QFN package with an exposed pad. Electrical performance is guaranteed over the extended temperature range of TC = -40°C to +85°C.

II. Manufacturing Information

A. Description/Function:	Dual, SiGe, High-Linearity, High-Gain, 700MHz to 1000MHz Down Conversion Mixer with LO Buffer/Switch
B. Process:	MFN SiGe HBT CMOS
C. Number of Device Transistors:	2863
D. Fabrication Location:	Oregon
E. Assembly Location:	UTL Thailand
F. Date of Initial Production:	7/25/2008

III. Packaging Information

A. Package Type:	36-pin TQFN 6x6
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2774
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	38°C/W
K. Single Layer Theta Jc:	1.4°C/W
L. Multi Layer Theta Ja:	28°C/W
M. Multi Layer Theta Jc:	1.4°C/W

IV. Die Information

A. Dimensions:	131 X 131 mils
B. Passivation:	Si_3N_4
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn) Metal 1, 2 & 3 5.6 microns (as drawn) Metal 4
F. Minimum Metal Spacing:	1.6 microns (as drawn) Metal 1, 2 & 3, 4.2 microns (as drawn) Metal 4
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are pending. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.4 \times 10^{-9}$

$\lambda = 22.4$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the G4 Process results in a FIT Rate of 0.2 @ 25C and 3.6 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The CR39-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000 V per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX19985AETX+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data