RELIABILITY REPORT

FOR

MAX1978ETM

PLASTIC ENCAPSULATED DEVICES

May 10, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Quality Assurance
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Conclusion

The MAX1978 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1978 is the smallest, safest, most accurate complete single-chip temperature controllers for Peltier thermoelectric cooler (TEC) modules. On-chip power FETs and thermal control-loop circuitry minimize external components while maintaining high efficiency. Selectable 500kHz/1MHz switching frequency and a unique ripple-cancellation scheme optimize component size and efficiency while reducing noise. Switching speeds of internal MOSFETs are optimized to reduce noise and EMI. An ultra-low-drift chopper amplifier maintains ±0.001°C temperature stability. Output current, rather than voltage, is directly controlled to eliminate current surges. Individual heating and cooling current and voltage limits provide the highest level of TEC protection.

The MAX1978 operates from a single supply and provides bipolar ±3A output by biasing the TEC between the outputs of two synchronous buck regulators. True bipolar operation controls temperature without "dead zones" or other nonlinearities at low load currents. The control system does not hunt when the set point is very close to the natural operating point, where only a small amount of heating or cooling is needed. An analog control signal precisely sets the TEC current

A chopper-stabilized instrumentation amplifier and a high-precision integrator amplifier are supplied to create a proportional-integral (PI) or proportional-integral-derivative (PID) controller. The instrumentation amplifier can interface to an external NTC or PTC thermistor, thermocouple, or semiconductor temperature sensor. Analog outputs are provided to monitor TEC temperature and current. In addition, separate overtemperature and undertemperature outputs indicate when the TEC temperature is out of range. An on-chip voltage reference provides bias for a thermistor bridge.

The MAX1978 is available in a low-profile 48-lead thin QFN-EP package and is specified over the -40°C to +85°C temperature range. The thermally enhanced QFN-EP package with exposed metal pad minimizes operating junction temperature. An evaluation kit is available to speed designs.

B. Absolute Maximum Ratings

Item	Rating
VDD to GND	-0.3V to +6V
SHDN, MAXV, MAXIP, MAXIN,CTLI, OT, UT to GND	-0.3V to +6V
FREQ, COMP, OS1, OS2, CS, REF, ITEC, AIN+, AIN-, AOUT, INT-, INTOUT, BFB+, BFB-, FB+, FB-, DIFOUT to GND	-0.3V to (VDD + 0.3V)
PVDD1, PVDD2 to VDD	-0.3V to +0.3V
PVDD1, PVDD2 to GND	-0.3V to (VDD + 0.3V)
PGND1, PGND2 to GND	-0.3V to +0.3V
COMP, REF, ITEC, OT, UT, INTOUT, DIFOUT, BFB-, BFB+, AOUT Short to GND	Indefinite
Peak LX Current (MAX1978) (Note 1)	±4.5A
Operating Temperature Range	-40°C to +85°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C) 48-Pin Thin QFN-EP	2105mW
Derates above +70°C (Note 2) 48-Pin Thin QFN-EP	26.3mW/°C

Note 1: LX has internal clamp diodes to PGND and PVDD. Applications that forward bias these diodes should not exceed the IC'spackage power dissipation limits.

Note 2: Solder underside metal slug to PC board ground plane.

II. Manufacturing Information

A. Description/Function:	Integrated Temperature Controllers for Peltier Modules
B. Process:	B8 (Standard 0.8 micron silicon gate CMOS)
C. Number of Device Transistors:	6023
D. Fabrication Location:	California, USA
E. Assembly Location:	Thailand
F. Date of Initial Production:	July, 2002

III. Packaging Information

A. Package Type:	4**8-Pin Thin QFN (7x7)**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (2 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-3501-0030
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1

IV. Die Information

A. Dimensions:	168 x 189 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations)
Bryan Preeshl (Managing Director**)**

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 135 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 8.04 \times 10^{-9}$

λ = 8.04 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5980) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the B8/S8 Process results in a FIT rate of 0.17 @ 25°C and 2.92 @ 55°C (eV = 0.8, UCL = 60%).

C. E.S.D. and Latch-Up Testing

The PM06-4 die type has been found to have all pins able to withstand a transient pulse of ±200V per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX1978ETM

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		135	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QFN	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

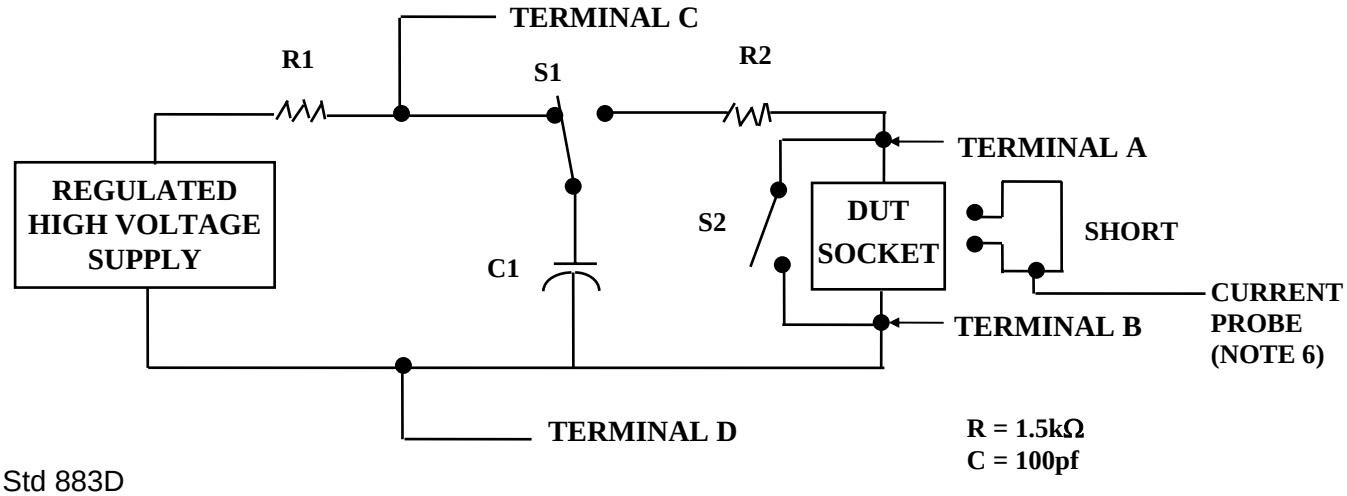
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

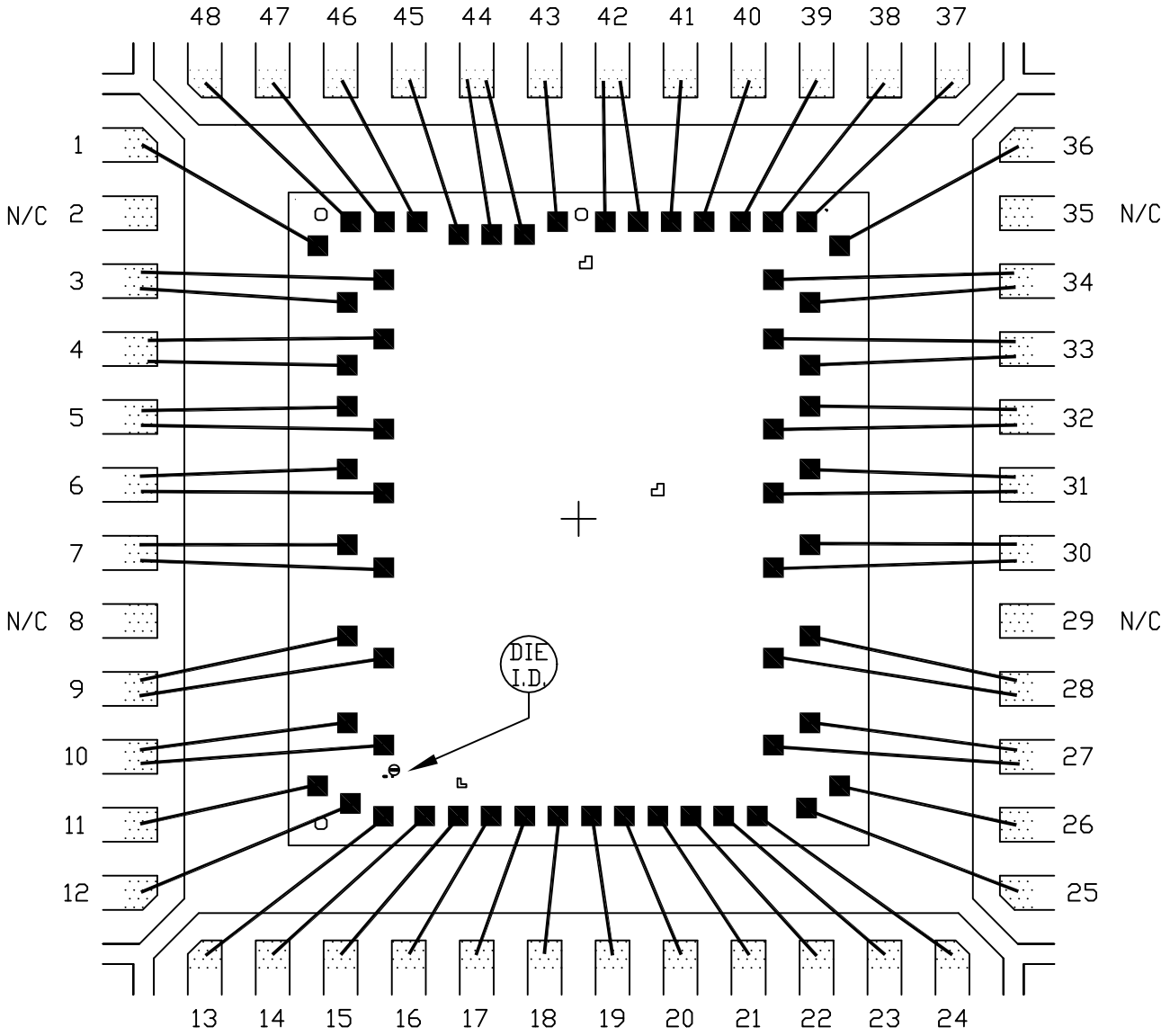
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

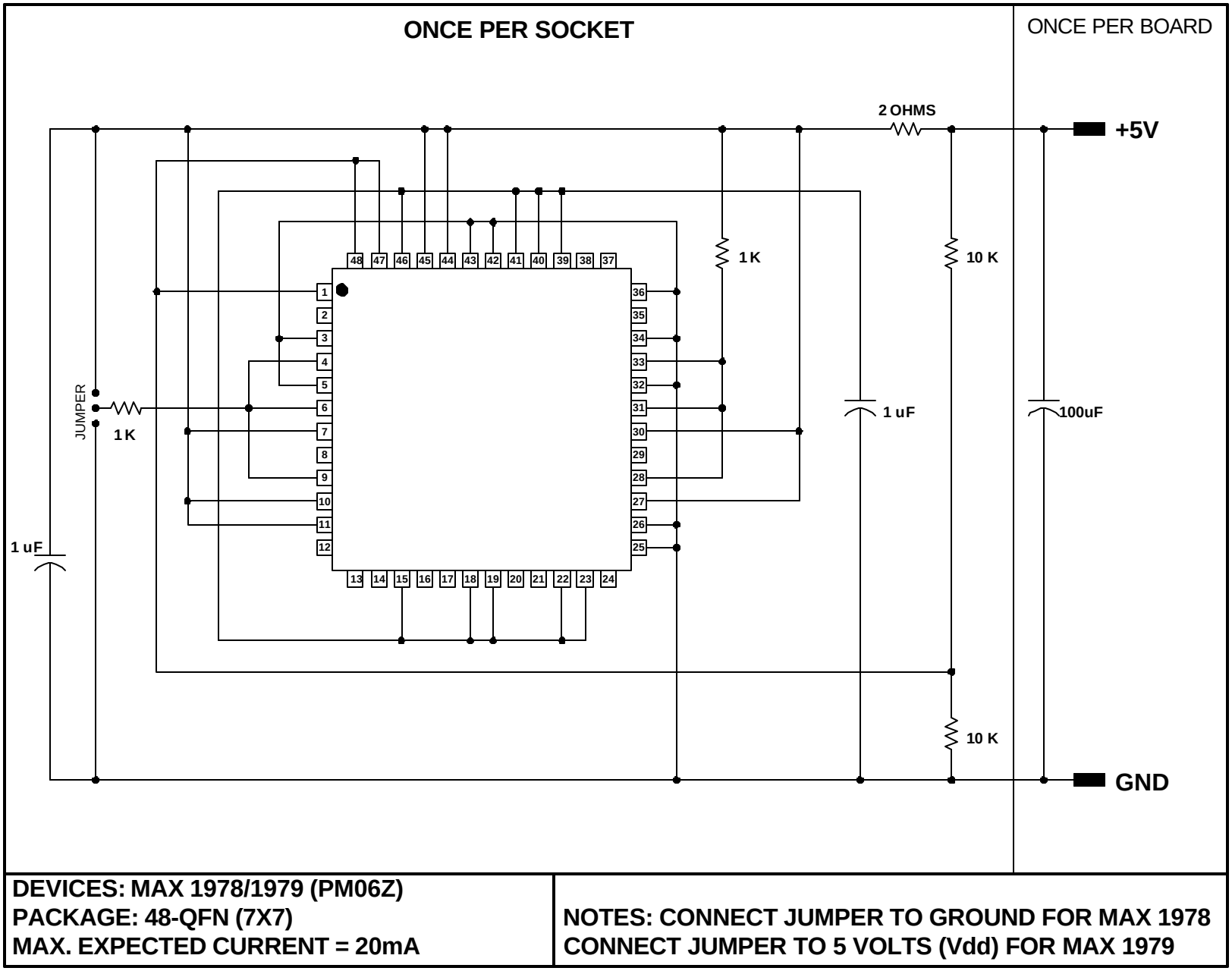


7x7x0.80mm THIN QFN PKG. EXPOSED PAD PKG.



BONDABLE AREA

PKG. CODE: T4877-6		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 228x228	PKG.			BOND DIAGRAM #: 05-3501-0030	REV: C
	DESIGN				



DEVICES: MAX 1978/1979 (PM06Z)
PACKAGE: 48-QFN (7X7)
MAX. EXPECTED CURRENT = 20mA

NOTES: CONNECT JUMPER TO GROUND FOR MAX 1978
CONNECT JUMPER TO 5 VOLTS (Vdd) FOR MAX 1979