RELIABILITY REPORT

FOR

MAX19705ETM+

PLASTIC ENCAPSULATED DEVICES

November 29, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX19705ETM+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX19705 is an ultra-low-power, mixed-signal analog front-end (AFE) designed for power-sensitive communication equipment. Optimized for high dynamic performance at ultra-low power, the device integrates a dual 10-bit, 7.5Msps receive (Rx) ADC; dual 10-bit, 7.5Msps transmit (Tx) DAC; three fast-settling 12-bit aux-DAC channels for ancillary RF front-end control; and a 10-bit, 333ksps housekeeping aux-ADC. The typical operating power in Tx-Rx FAST mode is 28.2mW at a 7.5MHz clock frequency. The Rx ADCs feature 55.1dB SNR and 73.4dBc SFDR at a 1.875MHz input frequency with a 7.5MHz clock frequency. The analog I/Q input amplifiers are fully differential and accept 1.024VP-P full-scale signals. Typical I/Q channel matching is ±0.01° phase and ±0.02dB gain. The Tx DACs feature 77.2dBc SFDR at fOUT = 620kHz and fCLK = 7.5MHz. The analog I/Q full-scale output voltage is ±400mV differential. The Tx DAC commonmode DC level is programmable from 0.9V to 1.35V. The I/Q channel offset is adjustable. The typical I/Q channel matching is ±0.03dB gain and ±0.08° phase. The Rx ADC and Tx DAC share a single, 10-bit parallel, high-speed digital bus allowing half-duplex operation for time-division duplex (TDD) applications. A 3-wire serial interface controls power-management modes, the aux-DAC channels, and the aux-ADC channels. The MAX19705 operates on a single +2.7V to +3.3V analog supply and +1.8V to +3.3V digital I/O supply. The MAX19705 is specified for the extended (-40°C to +85°C) temperature range and is available in a 48-pin, thin QFN package. See a parametric table of the complete family of pin-compatible AFEs.

II. Manufacturing Information

A. Description/Function:	10-bit, 7.5Msps, Ultra-Low-Power Analog Front-End
B. Process:	TS35
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Thailand
F. Date of Initial Production:	July 23, 2005

III. Packaging Information

A. Package Type:	48L TQFN 7x7
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1714 / A
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	36°C/W
K. Single Layer Theta Jc:	1°C/W
L. Multi Layer Theta Ja:	25°C/W
M. Multi Layer Theta Jc:	1°C/W

IV. Die Information

A. Dimensions:	143 X 163 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35µm
F. Minimum Metal Spacing:	0.35µm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS35 Process results in a FIT Rate of 0.11 @ 25C and 1.93 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot QJBABQ002B D/C 0525)

The CA21 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX19705ETM+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	QJBDAQ001B, D/C 0503

Note 1: Life Test Data may represent plastic DIP qualification lots.