RELIABILITY REPORT

FOR

MAX19700ETM+

PLASTIC ENCAPSULATED DEVICES

January 4, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

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Approved by
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Conclusion

The MAX19700ETM+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX19700 is an ultra-low-power, mixed-signal analog front-end (AFE) designed for TD-SCDMA handsets and data cards. Optimized for high dynamic performance at ultra-low power, the MAX19700 integrates a dual 10-bit, 7.5Msps receive (Rx) ADC, dual 10-bit, 7.5Msps transmit (Tx) DAC with TD-SCDMA baseband filters, and three fast-settling 12-bit aux-DAC channels for ancillary RF front-end control. The typical operating power in Tx-Rx FAST mode is 36.3mW at a 5.12Msps clock frequency. The Rx ADCs feature 54.9dB SINAD and 78dBc SFDR at a 1.87MHz input frequency with a 7.5Msps sample frequency. The analog I/Q input amplifiers are fully differential and accept 1.024VP-P full-scale signals. Typical I/Q channel matching is ±0.22° phase and ±0.02dB gain. The Tx DACs with TD-SCDMA lowpass filters feature -3dB cutoff frequency of 1.27MHz and >55dB stopband rejection at fIMAGE = 4.32MHz. The analog I/Q full-scale output voltage range is selectable at ±410mV or ±500mV. The output common-mode voltage is selectable from 0.9V to 1.4V and the I/Q channel offset is adjustable. The typical I/Q channel matching is ±0.05dB gain and ±0.16° phase. The Rx ADC and Tx DAC share a single, 10-bit parallel, high-speed digital bus allowing half-duplex operation for time-division duplex (TDD) applications. A 3-wire serial interface controls power-management modes and the aux-DAC channels. The MAX19700 operates on a single +2.7V to +3.3V analog supply and +1.8V to +3.3V digital I/O supply. The MAX19700 is specified for the extended (-40°C to +85°C) temperature range and is available in a 48-pin, thin QFN package. See a parametric table of the complete family of pin-compatible AFEs.

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II. Manufacturing Information

A. Description/Function:	7.5Msps, Ultra-Low-Power Analog Front-End
B. Process:	TS35
C. Number of Device Transistors:	
D. F abrication Location:	Taiwan
E. Assembly Location:	China, Thailand
F. Date of Initial Production:	January 22, 2005

III. Packaging Information

A. Package Type:	48-pin TQFN 7x7
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1713
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	36°C/W
K. Single Layer Theta Jc:	0.8°C/W
L. Multi Layer Theta Ja:	25°C/W
M. Multi Layer Theta Jc:	0.8°C/W

IV. Die Information

A. Dimensions:	143 X 163 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. B ackside Metallization:	None
E. Minimum Metal Width:	0.35μm F.
Minimum Metal Spacing:	0.35μm
G. Bondpad Dimensions:	5 mil. Sq.
H. I solation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. S ampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$

(Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

λ = 22.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS35 Process results in a FIT Rate of 0.11 @ 25C and 1.93 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot QJBDBA005A D/C 0611)

The CA21-3 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

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Table 1
Reliability Evaluation Test Results

MAX19700ETM+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	QJBDAQ001B, D/C 0503

Note 1: Life Test Data may represent plastic DIP qualification lots.

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