RELIABILITY REPORT

FOR

MAX19693EXW+

PLASTIC ENCAPSULATED DEVICES

September 10, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX19693EXW+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX19693 12-bit, 4.0Gsps digital-to-analog converter (DAC) enables direct digital synthesis of high-frequency and wideband signals. The DAC has been optimized for wideband communications and radar applications. The MAX19693 provides excellent spurious and noise performance and can be used for synthesis of wideband signals in the frequency range from DC to nearly 2GHz. The 4.0Gsps update rate enables digital synthesis of signals with more than 1.5GHz bandwidth.

The MAX19693 includes four 12-bit multiplexed low-voltage differential signaling (LVDS) input ports, each operating at up to 1GHz in double data rate (DDR) or quad data rate (QDR) mode. The DAC accepts a clock at 1/2 the DAC update rate, as conversion is triggered on both rising and falling clock edges. The input data rate is 1/4 the DAC update rate (1/2 the clock rate). The MAX19693 provides an LVDS data clock output to simplify interfacing to FPGA or ASIC devices.

The MAX19693 is a current-steering DAC with an integrated, self-calibrated 50Ù differential output termination to ensure optimum dynamic performance. The MAX19693 operates from 3.3V and 1.8V power supplies and consumes 1180mW at 4.0Gsps. The MAX19693 is specified over the extended temperature range (-40°C to +85°C) and is available in a compact 11mm x 11mm, 169 CSBGA package.

II. Manufacturing Information

A. Description/Function:	12-Bit, 4.0Gsps DAC Delivers -164dBm/Hz Noise Density at 1180mW
B. Process:	TS18
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Philippines
F. Date of Initial Production:	1/26/2008

III. Packaging Information

A. Package Type:	169-pin CSBGA
B. Lead Frame:	Substrate
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Au (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1369
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Multi Layer Theta Ja:	30°C/W
K. Multi Layer Theta Jc:	13°C/W

IV. Die Information

A. Dimensions:	203 X 250 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18µm
F. Minimum Metal Spacing:	0.18µm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 45 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 23.9 \times 10^{-9}$

λ = 23.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.24 @ 25C and 4.14 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The CD11-2 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500 V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1

Reliability Evaluation Test Results

MAX19693EXW+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data