RELIABILITY REPORT

FOR

MAX1964

PLASTIC ENCAPSULATED DEVICES

August 25, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by

Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX1964 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1964 power-supply controller ais designed to address cost-sensitive applications demanding voltage sequencing/tracking, such as cable modem consumer premise equipment (CPE), xDSL CPE, and set-top boxes. Operating off a low-cost, unregulated DC supply (such as a wall adapter output), the MAX1964 generates three positive outputs to provide an inexpensive system power supply.

The MAX1964 includes a current-mode synchronous step-down controller and two positive regulator gain blocks. The 200kHz operating frequency allows the use of low-cost aluminum-electrolytic capacitors and low-cost power magnetics. Additionally, the MAX1964 step-down controller sense the voltage across the low-side MOSFET's on-resistance to efficiently provide the current-limit signal, eliminating the need for costly current-sense resistors.

The MAX1964 generates additional supply rails at low cost. The positive regulator gain blocks use an external PNP pass transistor to generate low voltage rails directly from the main step-down converter (such as 2.5V or 1.8V from the main 3.3V output) or higher voltages using coupled windings from the step-down converter (such as 5V, 12V, or 15V).

All output voltages are externally adjustable, providing maximum flexibility. During startup, the MAX1964 features voltage and the controller provides a power-good output that monitors all of the output voltages.

B. Absolute Maximum Ratings

Item	Rating
IN,B2,B3,B4 to Gnd	-0.3V to +30V
B5 to OUT	-20V to +0.3V
VL, POK, FB, FB2, FB3, FB4, FB5 to Gnd	-0.3V to +6V
LX to BST	-6V to +0.3V
BST to Gnd	-0.3V to +36V
DH to LX	-0.3V to (VBST + 0.3V)
DL, OUT, COMP, ILIM to Gnd	-0.3V to (VL +0.3V)
VL Output Current	50mA
Operating Temperature Range	-40°C to +85°C
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
16-Pin QSOP	666mW
Derates above +70°C	
16-Pin QSOP	8.3mW/°C

II. Manufacturing Information

A. Description/Function: Tracking/Sequencing Triple Power-Supply Controller

B. Process: S8

C. Number of Device Transistors: 1617

D. Fabrication Location: Oregon, USA

E. Assembly Location: Korea, Philippines, Malaysia

F. Date of Initial Production: July, 2001

III. Packaging Information

A. Package Type:	**16-Pin QSOP**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-2301-0096
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions: 70 x 92 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: TiW/ AlCu/ TiWN

D. Backside Metallization: None

E. Minimum Metal Width: .8 microns (as drawn)

F. Minimum Metal Spacing: .8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Reliability Lab Manager)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83 \text{ (Chi square value for MTTF upper limit)}}{192 \times 4389 \times 80 \times 2}$$

(4389: Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.57 \times 10^{-9}$ $\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1L**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PY71-4 die type has been found to have all pins able to withstand a transient pulse of ±600V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±150mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX1964TEEE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QSOP	200	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the Small Outline package.
Note 2: Generic process/package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

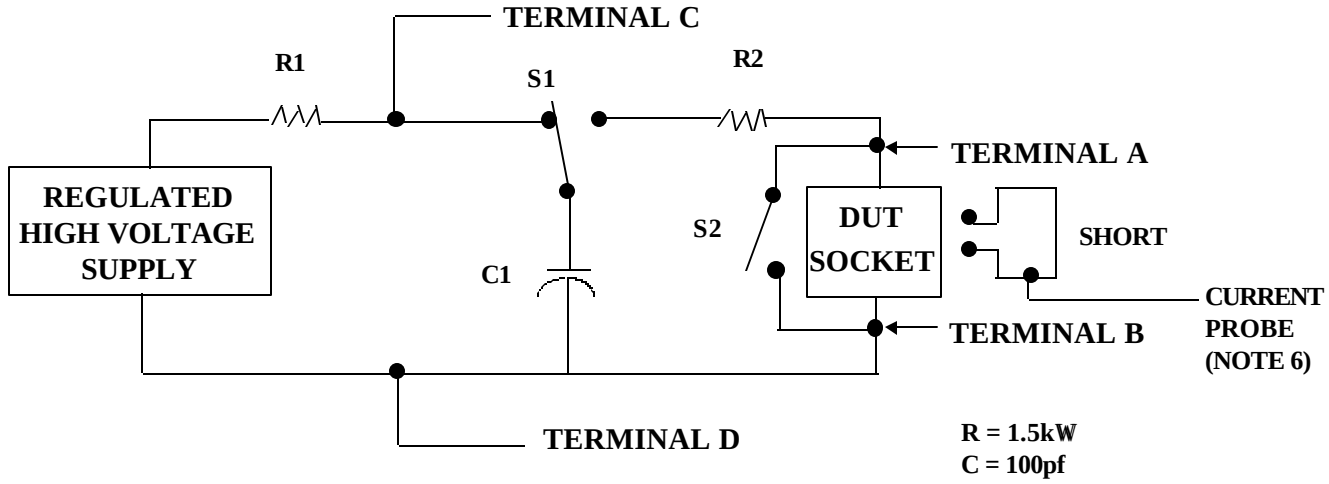
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

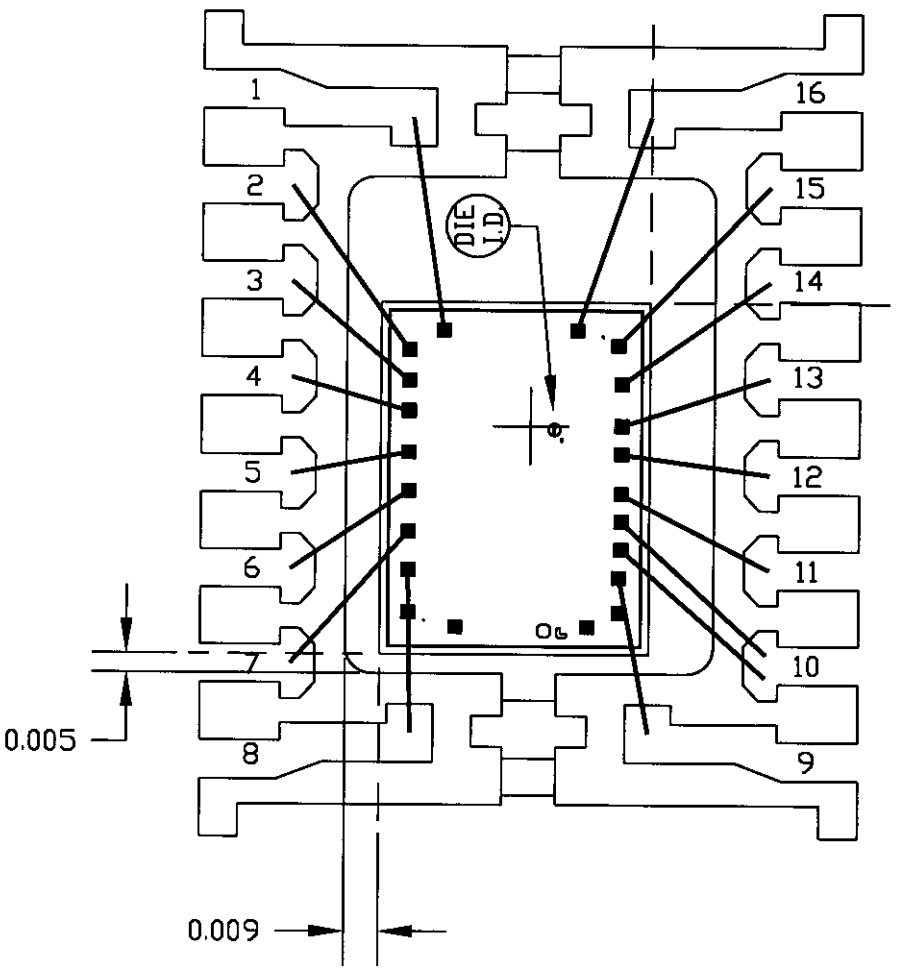
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG. CODE: E16-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 96X130	PKG. DESIGN			BOND DIAGRAM #: 05-2301-0096	REV: A