RELIABILITY REPORT

FOR

MAX19588ETN+D

PLASTIC ENCAPSULATED DEVICES

July 20, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX19588ETN+D successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX19588 is a 3.3V, high-speed, high-performance analog-to-digital converter (ADC) featuring a fully differential wideband track-and-hold (T/H) and a 16-bit converter core. The MAX19588 is optimized for multichannel, multimode receivers, which require the ADC to meet very stringent dynamic performance requirements. With a -82dBFS noise floor, the MAX19588 allows for the design of receivers with superior sensitivity requirements. At 100Msps, the MAX19588 achieves a 79dB signal-to-noise ratio (SNR) and an 82.1dBc/97.7dBc single-tone spurious-free dynamic range performance (SFDR1/SFDR2) at fIN = 70MHz. The MAX19588 is not only optimized for excellent dynamic performance in the 2nd Nyquist region, but also for high-IF input frequencies. For instance, at 130MHz, the MAX19588 achieves an 82.3dBc SFDR and its SNR performance stays flat (within 2.3dB) up to 175MHz. This level of performance makes the part ideal for high-performance digital receivers. The MAX19588 operates from a 3.3V analog supply voltage and a 1.8V digital voltage, features a 2.56VP-P full-scale input range, and allows for a guaranteed sampling speed of up to 100Msps. The input track-and-hold stage operates with a 600MHz full-scale, full-power bandwidth. The MAX19588 features parallel, low-voltage CMOS-compatible outputs in two's-complement output format. The MAX19588 is manufactured in an 8mm x 8mm, 56-pin thin QFN package with exposed paddle (EP) for low thermal resistance, and is specified for the extended industrial (-40°C to +85°C) temperature range.

II. Manufacturing Information

A. Description/Function:	High-Dynamic-Range, 16-Bit, 100Msps ADC with -82dBFS Noise Floor
B. Process:	TS18
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	China, Thailand
F. Date of Initial Production:	April 20, 2006

III. Packaging Information

A. Package Type:	56-pin TQFN 8x8
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1268
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	35°C/W
K. Single Layer Theta Jc:	0.6°C/W
L. Multi Layer Theta Ja:	21°C/W
M. Multi Layer Theta Jc:	0.6°C/W

IV. Die Information

A. Dimensions:	188 X 186 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18µm
F. Minimum Metal Spacing:	0.18µm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 144 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 7.6 \times 10^{-9}$

$\lambda = 7.6$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.24 @ 25C and 4.14 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The CA13-6 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX19588ETN+D

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	144	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data