RELIABILITY REPORT

FOR

MAX19515ETM+

PLASTIC ENCAPSULATED DEVICES

November 11, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX19515ETM+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX19515 dual-channel, analog-to-digital converter (ADC) provides 10-bit resolution and a maximum sample rate of 65Msps. The MAX19515 analog input accepts a wide 0.4V to 1.4V input common-mode voltage range, allowing DC-coupled inputs for a wide range of RF, IF, and baseband front-end components. The MAX19515 provides excellent dynamic performance from baseband to high input frequencies beyond 400MHz, making the device ideal for zero-intermediate frequency (ZIF) and high intermediate frequency (IF) sampling applications. The typical signal-to-noise ratio (SNR) performance is 60.1dBFS and typical spurious-free dynamic range (SFDR) is 82dBc at fIN = 70MHz and fCLK = 65MHz. The MAX19515 operates from a 1.8V supply. Additionally, an integrated, self-sensing voltage regulator allows operation from a 2.5V to 3.3V supply (AVDD). The digital output drivers operate on an independent supply voltage (OVDD) over the 1.8V to 3.5V range. The analog power consumption is only 43mW per channel at V AVDD = 1.8V. In addition to low operating power, the MAX19515 consumes only 1mW in power-down mode and 15mW in standby mode. Various adjustments and feature selections are available through programmable registers that are accessed through the 3-wire serial-port interface. Alternatively, the serial-port interface can be disabled, with the three pins available to select output mode, data format, and clock-divider mode. Data outputs are available through a dual parallel CMOS-compatible output data bus that can also be configured as a single multiplexed parallel CMOS bus. The MAX19515 is available in a small 7mm x 7mm 48-pin thin QFN package and is specified over the -40°C to +85°C extended temperature range. Refer to the MAX19505, MAX19506, and MAX19507 data sheets for pin- and feature-compatible 8-bit, 65Msps, 100Msps, and 130Msps versions, respectively. Refer to the MAX19516 and MAX19517 data sheets for pin- and feature-compatible 10-bit, 100Msps and 130Msps versions, respectively.

II. Manufacturing Information

A. Description/Function:	Dual-Channel, 10-Bit, 65Msps ADC
B. Process:	TS18
C. Number of Device Transistors:	467602
D. Fabrication Location:	Taiwan
E. Assembly Location:	China and Thailand
F. Date of Initial Production:	July 25, 2008

III. Packaging Information

A. Package Type:	48-pin TQFN 7x7
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3205
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	36°C/W
K. Single Layer Theta Jc:	1°C/W
L. Multi Layer Theta Ja:	25°C/W
M. Multi Layer Theta Jc:	1°C/W

IV. Die Information

A. Dimensions:	146 X 138 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18µm
F. Minimum Metal Spacing:	0.18µm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Operations) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.24 @ 25C and 4.14 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot QJKZCQ001D, D/C 1026)

The CA24 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2500V per JEDEC JESD22-A114
ESD-CDM:	+/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/- 100mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX19515ETM+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	QJKZBQ001C, D/C 0810

Note 1: Life Test Data may represent plastic DIP qualification lots.