

RELIABILITY REPORT  
FOR  
**MAX191xxxG**  
PLASTIC ENCAPSULATED DEVICES

April 18, 2003

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

A handwritten signature in black ink, appearing to read "J Pedicord".

Jim Pedicord  
Quality Assurance  
Reliability Lab Manager

Reviewed by

A handwritten signature in black ink, appearing to read "Bryan J. Preeshl".

Bryan J. Preeshl  
Quality Assurance  
Executive Director

## Conclusion

The MAX191 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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## I. Device Description

### A. General

The MAX191 is a monolithic, CMOS, 12-bit analog-to-digital converter (ADC) featuring differential inputs, track/hold (T/H), internal voltage reference, internal or external clock, and parallel or serial  $\mu$ P interface. The MAX191 has a 7.5 $\mu$ s conversion time, a 2 $\mu$ s acquisition time, and a guaranteed 100ksps sample rate.

The MAX191 operates from a single +5V supply or from dual  $\pm$ 5V supplies, allowing ground-referenced bipolar input signals. The device features a logic power-down input, which reduces the 3mA VDD supply current to 50 $\mu$ A max, including the internal-reference current.

Decoupling capacitors are the only external components needed for the power supply and reference. This ADC operates with either an external reference, or an internal reference that features an adjustment input for trimming system gain errors.

The MAX191 provides three interface modes: two 8-bit parallel modes, and a serial interface mode that is compatible with SPI™, QSPI™, and MICROWIRE™ serial-interface standards.

### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
VDD to DGND	-0.3V to +7V
VSS to AGND	-7V to +0.3V
VDD to VSS	12V
AGND, VREF, REFADJ to DGND	-0.3V to (VDD + 0.3V)
AIN+, AIN-, PD to VSS	-0.3V to (VDD + 0.3V)
CS, RD, CLK, BIP, HBEN, PAR, to DGND	-0.3V to (VDD + 0.3V)
BUSY, D0–D7 to DGND	-0.3V to (VDD + 0.3V)
Operating Temperature Ranges	
MAX191_C_ _	0°C to +70°C
MAX191_E_ _	-40°C to +85°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10sec)	+300°C
Continuous Power Dissipation (TA = +70°C)	
24-Pin WSO	941mW
24-Pin Narrow PDIP	1067mW
Derates above +70°C	
24-Pin WSO	11.76mW/°C
24-Pin Narrow PDIP	13.33mW/°C

## II. Manufacturing Information

A. Description/Function:	Low-Power, 12-Bit Sampling ADC with Internal Reference and Power-Down
B. Process:	SG5 (Standard 5 micron silicon gate CMOS)
C. Number of Device Transistors:	1761
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines
F. Date of Initial Production:	September, 1992

## III. Packaging Information

A. Package Type:	<b>24-Lead WSO</b>	<b>24-Lead PDIP</b>
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0101-0335	# 05-0101-0333
H. Flammability Rating:	Class UL94-V0	Class UL94-V0

## IV. Die Information

A. Dimensions:	142 x 198 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	5 microns (as drawn)
F. Minimum Metal Spacing:	5 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

### A. Quality Assurance Contacts:

Jim Pedicord	(Manager, Rel Operations)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{6.21}{192 \times 4389 \times 971 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Thermal acceleration factor assuming a 0.8eV activation energy

$$\lambda = 3.79 \times 10^{-9} \quad \lambda = 3.79 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. # 06-2888) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The AD44-1 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2000\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 100\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX191xxxG**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		971	2
<b>Moisture Testing</b> (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	WSO	77	0
			PDIP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
<b>Mechanical Stress</b> (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

## Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ 3/	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

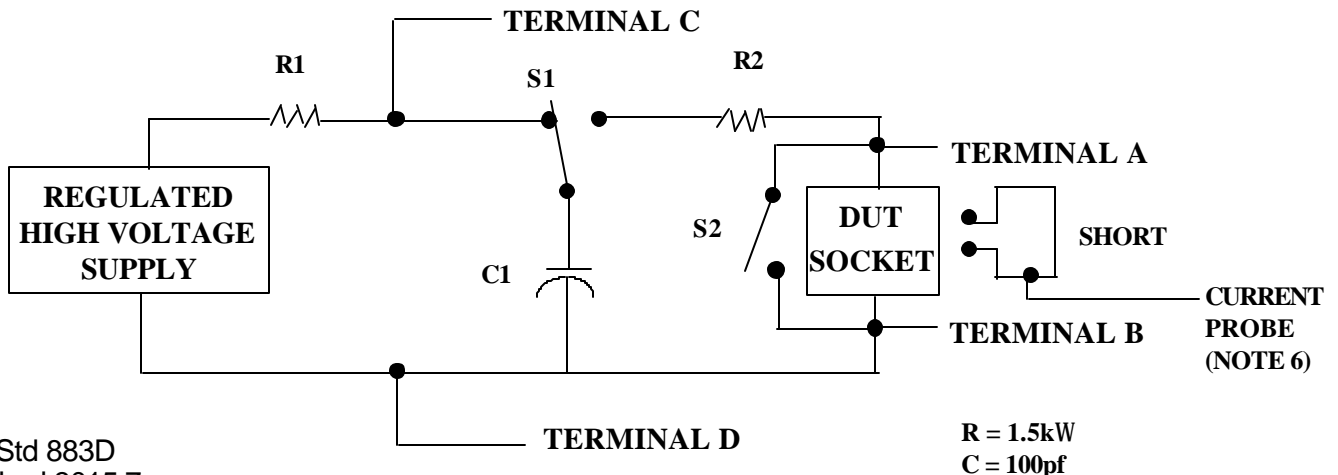
2/ No connects are not to be tested.

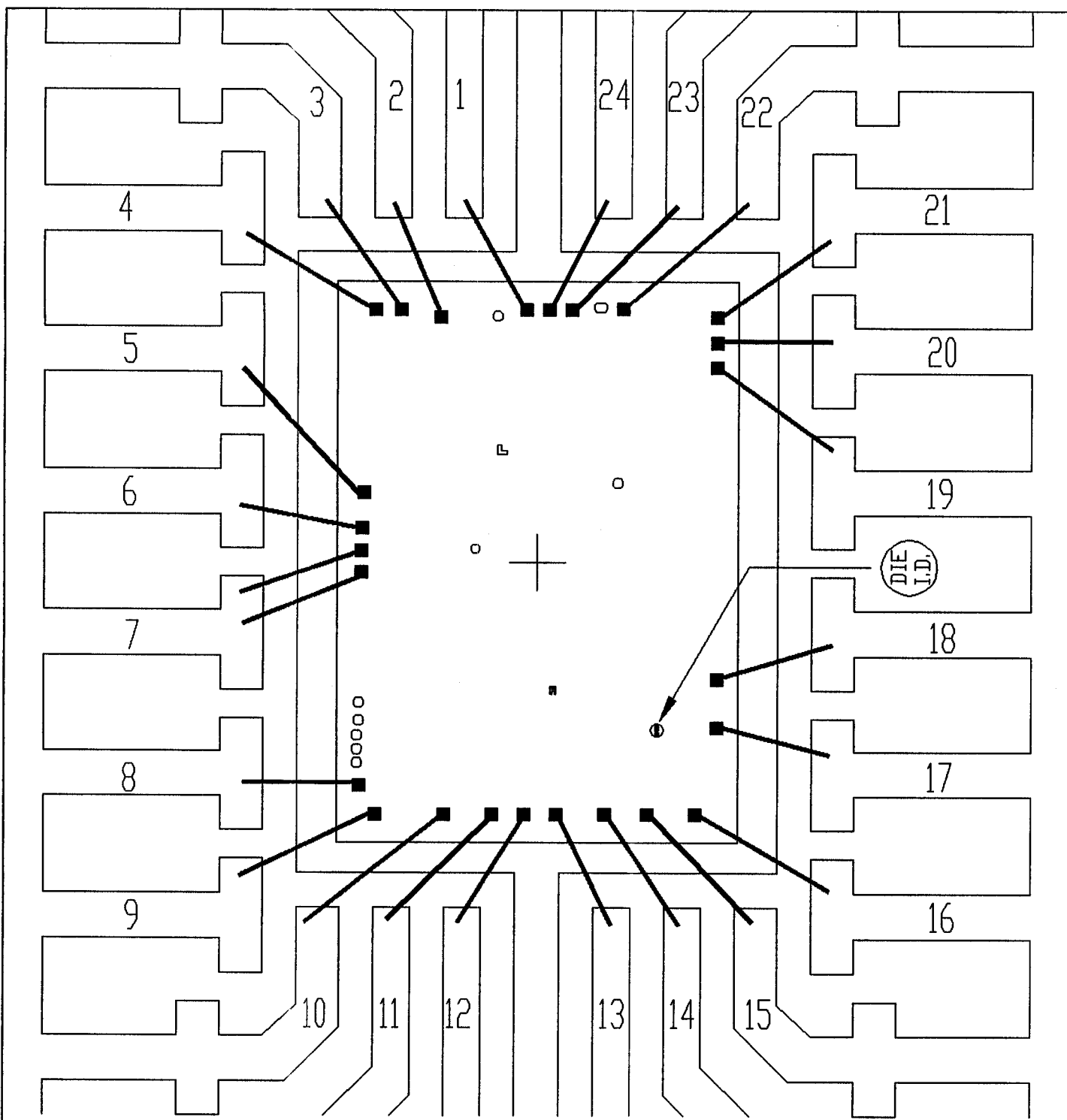
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

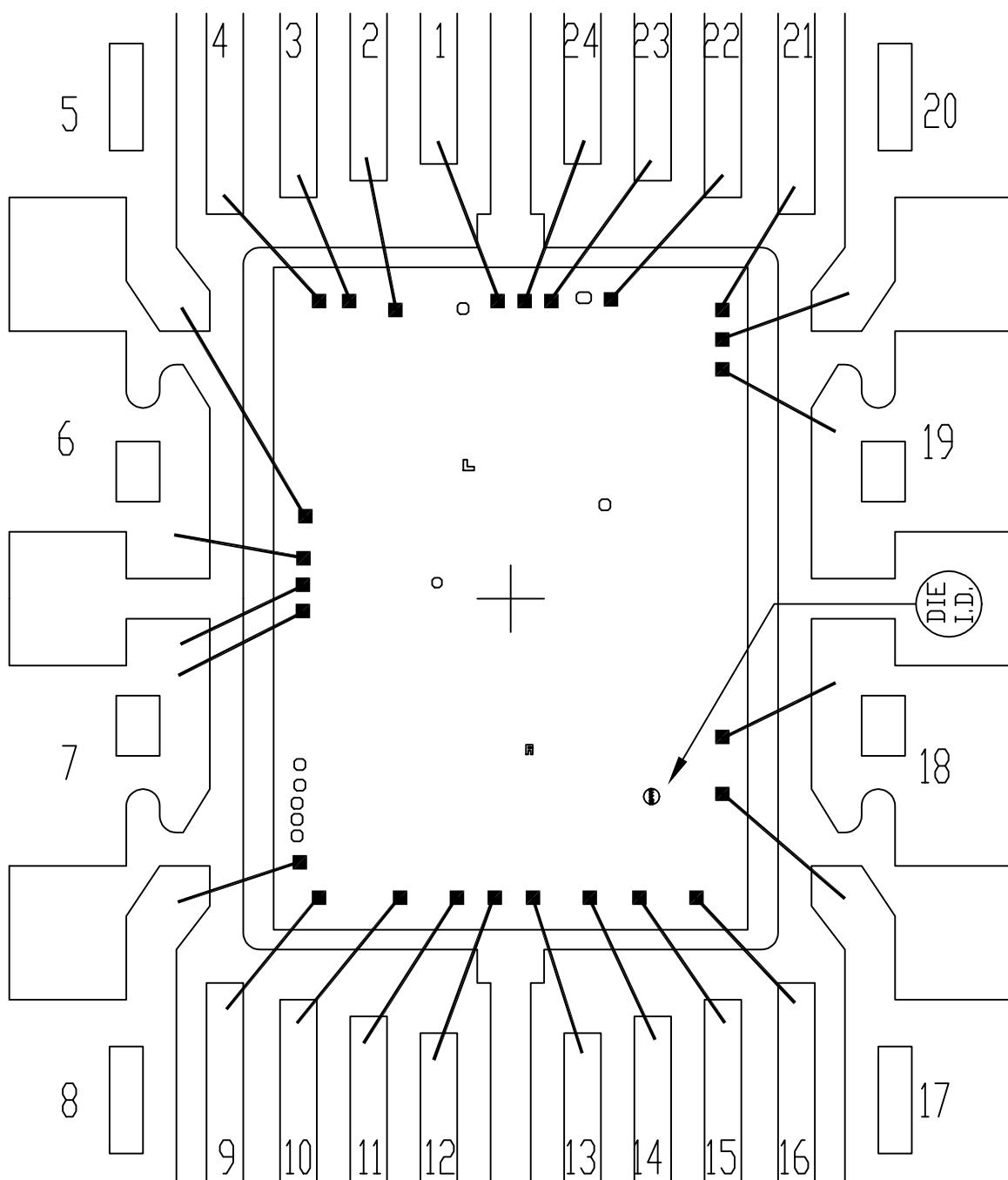
### 3.4 Pin combinations to be tested.

- Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



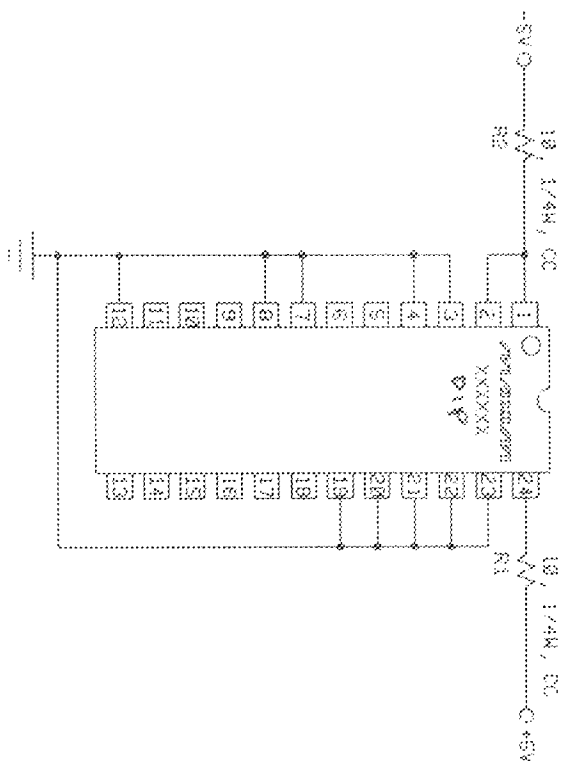


PKG.CODE: W24-2		APPROVALS	DATE	<b>MAXIM</b>	
CAV./PAD SIZE: 170 X 220	PKG. DESIGN			BUILDSHEET NUMBER: 05-0101-0335	REV.: A

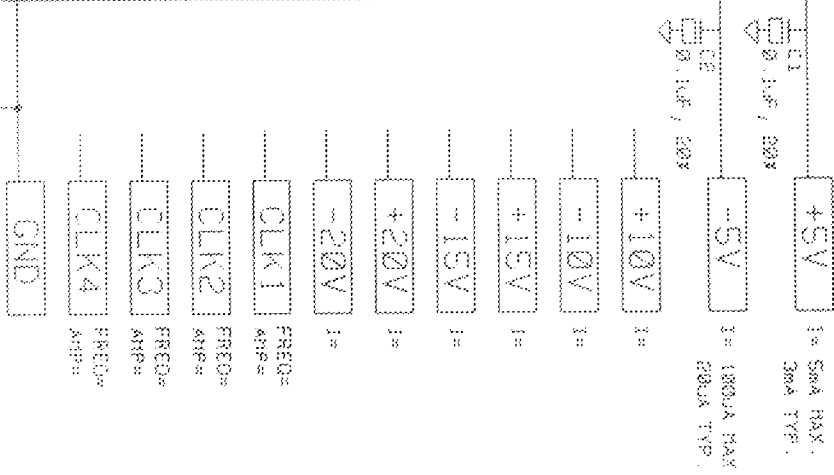


PKG. CODE: N24-3		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 160x210	PKG. DESIGN			BOND DIAGRAM #: 05-0101-0333	REV: B

ONCE PER SOCKET



ONCE PER BOARD



--STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.  
--BURN-IN IS PER MIL-STD-883 METHOD 1015. COND. B OR C

# NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 168 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 125C CONDITIONS
4. APPROVED FOR (X) COMMERCIAL (X) HS/800

SPEC. NO. 05-2888 REV. A

MAXIM BURN-IN SCHEMATIC

DATE: 5/27/92

DEVICE TYPE:  
MAX1867/1

DRAWN BY: