

RELIABILITY REPORT  
FOR  
**MAX1795EUA**  
PLASTIC ENCAPSULATED DEVICES

June 6, 2002

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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## Conclusion

The MAX1795 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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## I. Device Description

### A. General

The MAX1795 is a high efficiency step-up DC-DC converter intended for small portable hand-held devices. This devices feature Maxim's True-Shutdown™ circuitry, which fully disconnects the output from the input in shutdown, improves efficiency, and eliminates costly external components. The device also feature Maxim's proprietary LX-damping circuitry for reduced EMI in noise-sensitive applications. For additional in-system flexibility, a battery monitoring comparator (LBI/LBO) remains active even when the DC-DC converter is in shutdown.

The input voltage range is +0.7V to  $V_{OUT}$ , where  $V_{OUT}$  can be set from +2V to +5.5V. Startup is guaranteed from +0.85V. The MAX1795 has a preset, pin-selectable 5V or 3.3V output. The output can also be adjusted to other voltages, using two external resistors. The MAX1796 has a current limits of 0.25A and is packaged in a compact 8-pin  $\mu$ MAX package that is only 1.09mm tall and half the size of an 8-pin SO.

### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
OUT, LX, SHDN, LBI, LBO, BATT to GND	-0.3V to +6V
Output Short-Circuit Duration	5s
Junction Temperature	+150°C
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
8-Pin $\mu$ Max	330mW
Derates above +70°C	
8-Pin $\mu$ Max	4.1mW/°C

## II. Manufacturing Information

A. Description/Function:	Low Supply Current, Step-Up DC-DC Converter
B. Process:	S8 - Standard .8 micron silicon gate CMOS
C. Number of Device Transistors:	1100
D. Fabrication Location:	California, USA
E. Assembly Location:	Malaysia or Philippines
F. Date of Initial Production:	October, 2000

## III. Packaging Information

A. Package Type:	<b>8-Lead uMax</b>
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-2301-0028
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

## IV. Die Information

A. Dimensions:	61 x 82 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Si
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 155 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

↑  
Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 7.01 \times 10^{-9} \quad \lambda = 7.01 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5639) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1L**).

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The PY16 die type has been found to have all pins able to withstand a transient pulse of  $\pm 400\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 50\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX1795EUA**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	155	0
<b>Moisture Testing</b> (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	117	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
<b>Mechanical Stress</b> (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters (generic test vehicle)	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic Process/Package data

# Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ 3/	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

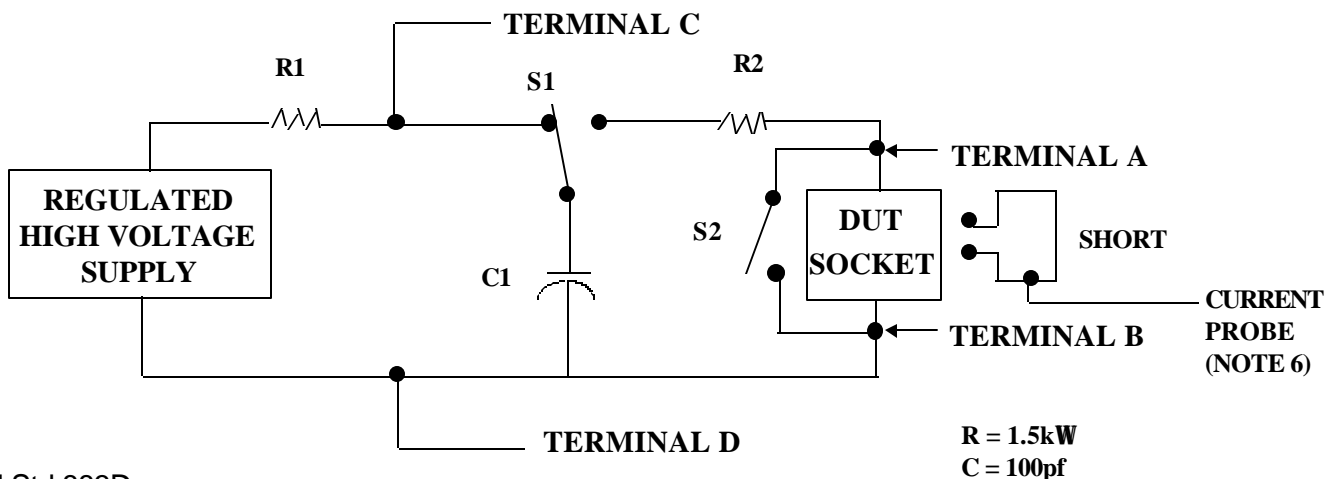
2/ No connects are not to be tested.

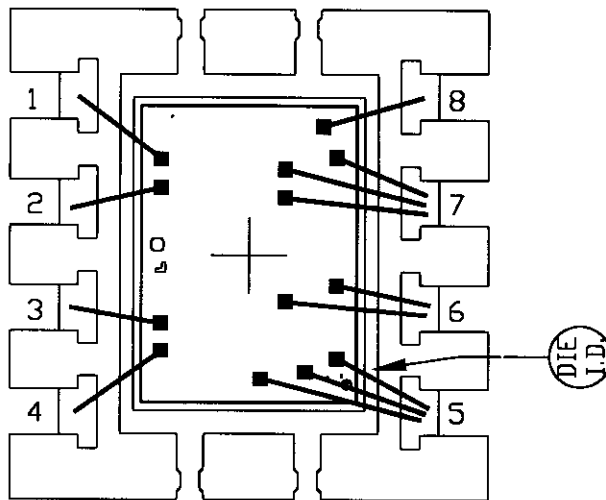
3/ Repeat pin combination I for each named Power supply and for ground


(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

## 3.4 Pin combinations to be tested.

- Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

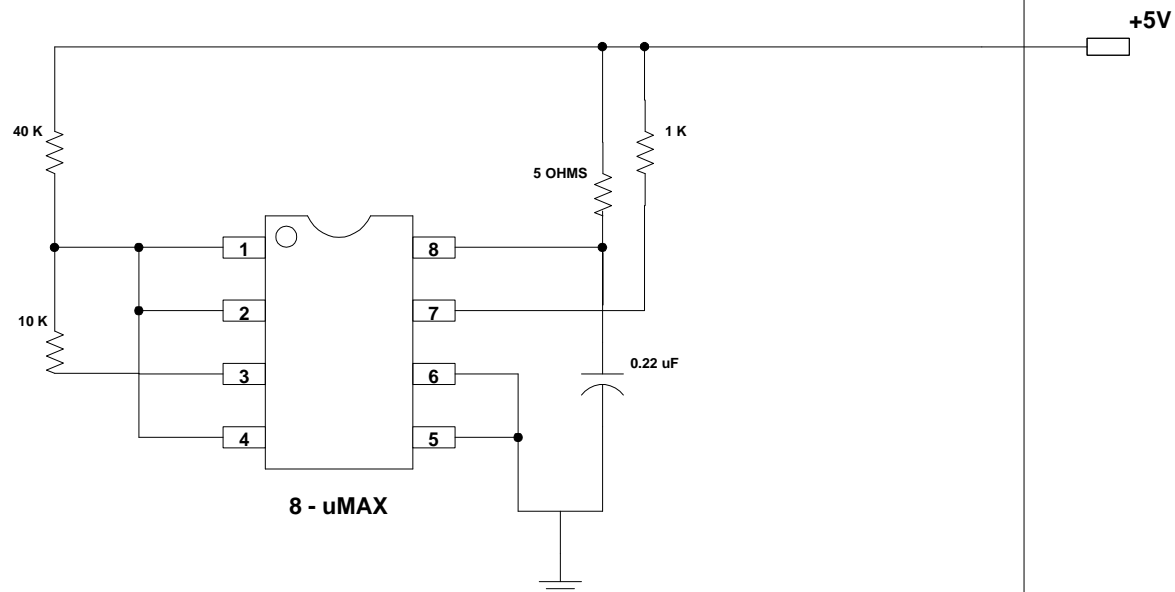




PKG.CODE:	U8-1		APPROVALS	DATE		
CAV./PAD SIZE:	68X94	PKG.			BUILDSHEET NUMBER:	REV:
		DESIGN			05-2301-0028	A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 1795/1796/1797

MAX. EXPECTED CURRENT = 10 mA

DRAWN BY: HAK TAN

NOTES: