RELIABILITY REPORT

FOR

MAX1772EEI

PLASTIC ENCAPSULATED DEVICES

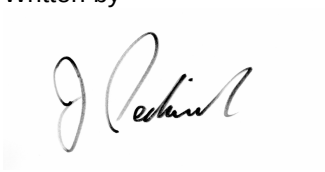
April 16, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



Jim Pedicord
Quality Assurance
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Quality Assurance
Executive Director

Conclusion

The MAX1772 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1772 is a highly-integrated, multichemistry battery-charger control IC that simplifies the construction of accurate and efficient chargers. The MAX1772 uses analog inputs to control charge current and voltage and can be programmed by the host or hardwired. High efficiency is achieved by a buck topology with synchronous rectification.

Maximum current drawn from the AC adapter is programmable to avoid overloading the AC adapter when supplying the load and the battery charger simultaneously. This enables the user to reduce the cost of the AC adapter. The MAX1772 provides outputs that can be used to monitor the current drawn from the AC adapter, battery-charging current, and the presence of an AC adapter.

The MAX1772 can charge two to four lithium-ion (Li+) series cells, easily providing 4A. When charging, the MAX1772 automatically transitions from regulating current to regulating voltage. It is available in a space-saving 28-pin QSOP package.

B. Absolute Maximum Ratings

Item	Rating
DCIN, CSSP, CSSN to GND	-0.3V to +30V
BST to GND	-0.3V to +36V
BST to LX	-0.3V to +6V
DHI to LX	-0.3V to (BST + 0.3V)
LX to GND	-6V to +30V
BATT, CSIP, CSIN to GND	-0.3V to 20V
CSIP to CSIN or CSSP to CSSN or PGND to GND	-0.3V to +0.3V
CCI, CCS, CCV, DLO, ICHG, IINP, ACIN, REF to GND	-0.3V to (VLDO + 0.3V)
DLOV to LDO	-0.3V to +0.3V
DLO to PGND	-0.3V to (DLOV + 0.3V)
LDO Short-Circuit Current	50mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	150°C
Storage Temperature Range	-60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C0	
28-Pin QSOP	860mW
Derates above +70°C	
28-Pin QSOP	10.8mW/°C

II. Manufacturing Information

A. Description/Function:	Low-Cost, Multichemistry Battery-Charger Building Block
B. Process:	S12 - Standard 1.2 micron silicon gate CMOS
C. Number of Device Transistors:	2733
D. Fabrication Location:	California or Oregon, USA
E. Assembly Location:	Thailand, Malaysia or Philippines
F. Date of Initial Production:	July, 2000

III. Packaging Information

A. Package Type:	2**8-Lead QSOP**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1101-0155
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	160 x 86 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 160 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 6.79 \times 10^{-9}$ $\lambda = 6.79$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5711) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PX85 die type has been found to have all pins able to withstand a transient pulse of ±200V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX1772EEI

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	160	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Process/Package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

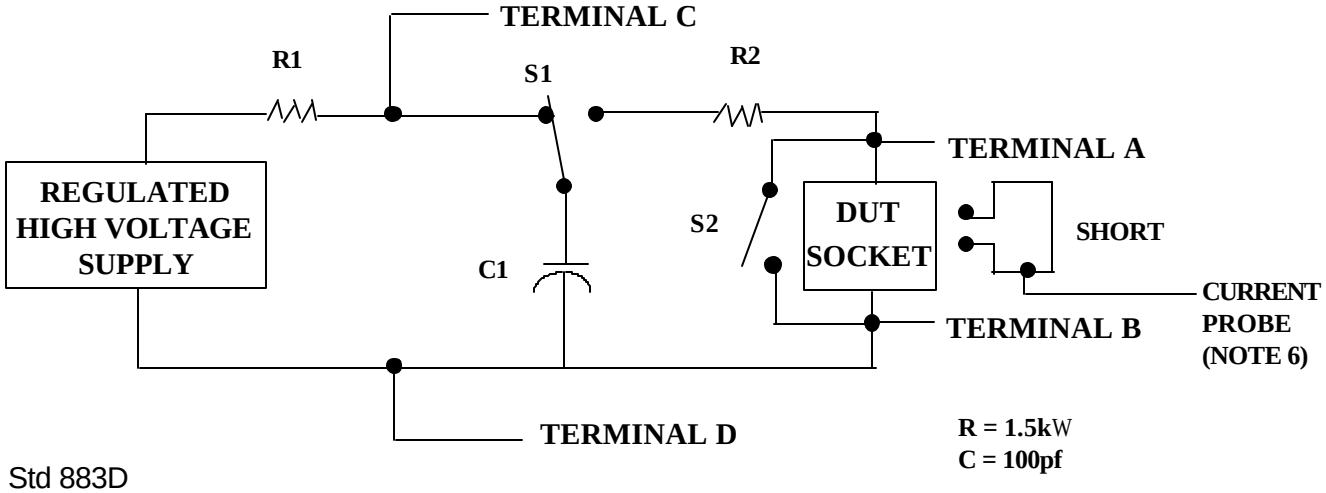
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

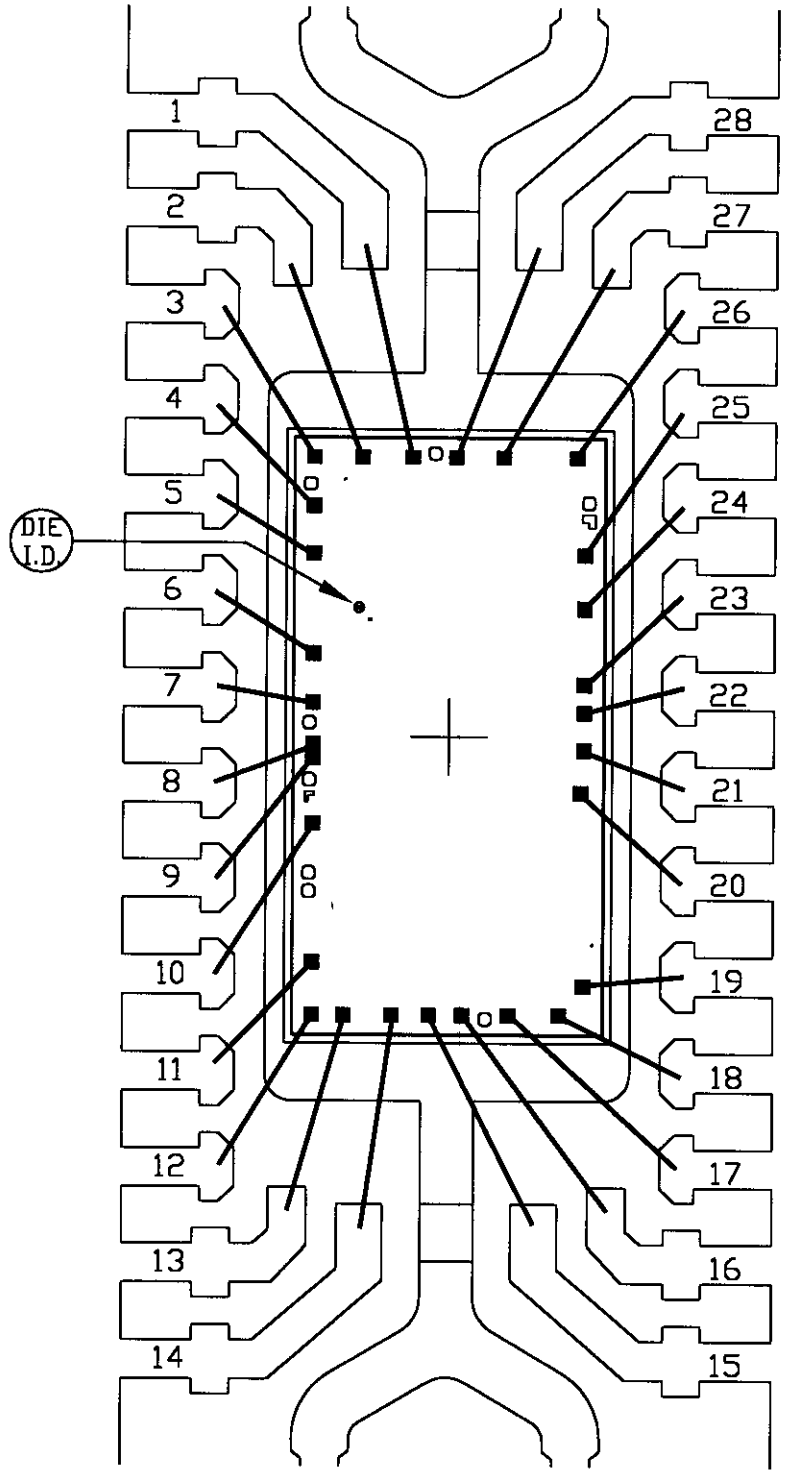
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

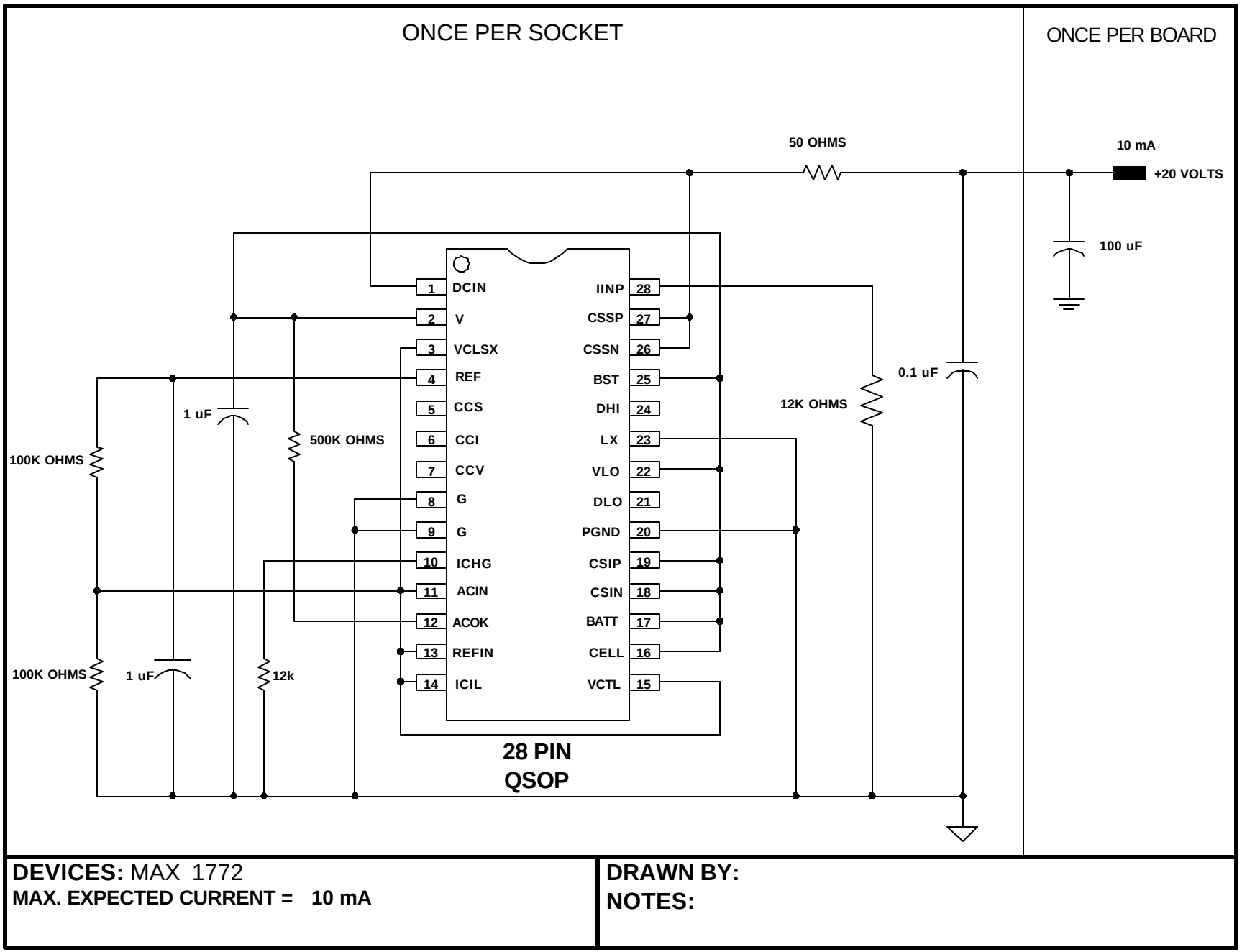
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8



PKG. CODE: E28-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 96X190	PKG. DESIGN			BOND DIAGRAM #: 05-1101-0155	REV: A



DEVICES: MAX 1772
MAX. EXPECTED CURRENT = 10 mA

DRAWN BY:
NOTES: