RELIABILITY REPORT FOR

MAX17552AUB+T / MAX17552ATB+T

PLASTIC ENCAPSULATED DEVICES

May 9, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Eric Wright
Quality Assurance
Reliability Engineering

Conclusion

The MAX17552AUB+T / MAX17552ATB+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX17552 high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over a 4V to 60V input voltage range. The converter can deliver output current up to 100mA at output voltages of 0.8V to 0.9 x VIN. The output voltage is accurate to within ±1.75% over the -40°C to +125°C temperature range. The device employs a peak-current-mode control architecture with a MODE pin that can be used to operate the device in pulse-width modulation (PWM) or pulse- frequency modulation (PFM) control schemes. PWM operation provides constant frequency operation at all loads and is useful in applications sensitive to variable switching frequency. PFM operation disables negative inductor current and additionally skips pulses at light loads for high efficiency. The converter consumes only 22pA of no-load supply current in PFM mode. The low-resistances, on-chip MOSFETs ensure high efficiency at full load and simplify PCB layout. The device offers programmable switching frequency to optimize solution size and efficiency. Programmable soft-start allows the user to reduce the inrush currents. An EN/UVLO pin allows the user to turn on/off the device at the desired input-voltage level. An open-drain RESET pin allows output-voltage monitoring. The device operates over the -40°C to +125°C industrial temperature range and is available in a compact 10-pin (3mm x 2mm) TDFN and 10-pin (3mm x 3mm) µMAX packages. Simulation models are available.

II. Manufacturing Information

A. Description/Function:	60V, 100mA, Ultra-Small, High-Efficiency, Synchronous Step-Down DC-DC Converter with 22uA No-Load Supply Current	
B. Process:	S18	
C. Number of Device Transistors:	22440	
D. Fabrication Location:	Japan	
E. Assembly Location:	Philippines, Thailand	Taiwan, Thailand
F. Date of Initial Production:	March 28, 2014	

III. Packaging Information

A. Package Type:	10-pin µMAX	10-pin TDFN
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Nickel	NiPdAu
D. Die Attach:	Conductive	Non-conductive
E. Bondwire:	Au (1.3 mil dia.)	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5334	#05-9000-5331
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	180°C/W	87.5°C/W
K. Single Layer Theta Jc:	42°C/W	18.2°C/W
L. Multi Layer Theta Ja:	113.1°C/W	67.3°C/W
M. Multi Layer Theta Jc:	42°C/W	18.2°C/W

IV. Die Information

A. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
B. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
C. Backside Metallization:	None
D. Minimum Metal Width:	0.23 microns (as drawn)
E. Minimum Metal Spacing:	0.23 microns (as drawn)
F. Bondpad Dimensions:	
G. Isolation Dielectric:	SiO_2
H. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 75 \times 2}$$

(Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 14.7 \times 10^{-9}$

λ = 14.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25°C and 0.93 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot EAQK7Q003B, D/C 1435)

The PI24-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114.

Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78
With the following exceptions:

EN/UVLO pin passes +100mA/-75mA per JEDEC JESD78
RESETB pin passes +100mA/-65mA per JEDEC JESD78

Table 1
Reliability Evaluation Test Results

MAX17552AUB+T / MAX17552ATB+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	75	0	EAQK7Q003E, D/C 1345

Note 1: Life Test Data may represent plastic DIP qualification lots.