

RELIABILITY REPORT FOR MAX17523ATE+ PLASTIC ENCAPSULATED DEVICES

March 1, 2017

# **MAXIM INTEGRATED**

160 RIO ROBLES SAN JOSE, CA 95134

Eric Wright Reliability Engineer

Brian Standley Manager, Reliability



## Conclusion

The MAX17523ATE+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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#### I. Device Description

A. General

The MAX17523 adjustable overvoltage and overcurrent protection device is ideal for protecting systems against positive and negative input voltage faults up to  $\pm$ 40V, and feature low 190m (typ) R<sub>oN</sub> integrated FETs.

The adjustable overvoltage range is between 6V and 36V, while the adjustable undervoltage range is between 4.5V and 24V. The overvoltage-lockout (OVLO) and undervoltage-lockout (UVLO) thresholds are set using optional external resistors. The factory preset internal OVLO threshold is 33V (typ), and the preset internal UVLO threshold is 19V (typ).

The MAX17523 also features programmable current-limit protection up to 1A. The device can be set for autoretry, latch-off, or continuous fault response when an overcurrent event occurs. Once current reaches the threshold, the MAX17523 turns off after 21ms (typ) blanking time, and stays off during the retry period when set to autoretry mode. The device latches off after the blanking time when set to latch-off mode. The device limits the current continuously when set to continuous mode. The MAX17523 also features reverse current and thermal shutdown protection.

The MAX17523 is available in a small, 16-pin (3mm x 3mm) TQFN package. The MAX17523 operates over the -40°C to +125°C extended temperature range.



## II. Manufacturing Information

A. Description/Function:	1A Adjustable Overcurrent and Overvoltage Protector with High Accuracy
B. Process:	S18
C. Number of Device Transistors:	4700
D. Fabrication Location:	USA
E. Assembly Location:	Taiwan

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## III. Packaging Information

F. Date of Initial Production:

A. Package Type:	16-pin TQFN
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Cu (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5566
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	68°C/W
K. Single Layer Theta Jc:	10°C/W
L. Multi Layer Theta Ja:	48°C/W
M. Multi Layer Theta Jc:	10°C/W

# IV. Die Information

A. Dimensions:	68.8976X68.8976 mils
B. Passivation:	$Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	AI/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Isolation Dielectric:	SiO <sub>2</sub>
H. Die Separation Method:	Wafer Saw



## V. Quality Assurance Information

Α.	Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)
В.	Outgoing Inspection Level:	<ul><li>0.1% for all electrical parameters guaranteed by the Datasheet.</li><li>0.1% for all Visual Defects.</li></ul>
C.	Observed Outgoing Defect Rate:	< 50 ppm
D.	Sampling Plan:	Mil-Std-105D

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

 $\lambda = \underbrace{1}_{\text{MTTF}} = \underbrace{1.83}_{\text{192 x 4340 x 78 x 2}} \text{ (Chi square value for MTTF upper limit)}_{\text{(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)}$  $\lambda = 14.1 \times 10^{-9}$ 

x = 14.1 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

## B. E.S.D. and Latch-Up Testing

The AL26-1 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.



# Table 1 Reliability Evaluation Test Results

## MAX17523ATE+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS	
Static Life Test (Note 1)						
	Ta = 135C	DC Parameters	78	0		
	Biased	& functionality				
	Time = 192 hrs.					

Note 1: Life Test Data may represent plastic DIP qualification lots.