RELIABILITY REPORT FOR

MAX17503ATP+T / MAX17504ATP+T / MAX17505ATP+T

PLASTIC ENCAPSULATED DEVICES

May 9, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX17503ATP+T / MAX17504ATP+T / MAX17505ATP+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX17503 high-efficiency, high-voltage, synchronously rectified step-down converter with dual integrated MOSFETs operates over a 4.5V to 60V input. It delivers up to 2.5A and 0.9V to 90%VIN output voltage. Built-in compensation across the output voltage range eliminates the need for external components. The feedback (FB) regulation accuracy over -40°C to +125°C is ±1.1%. The device is available in a compact (4mm x 4mm) TQFN lead (Pb)-free package with an exposed pad. Simulation models are available. The device features a peak-current-mode control architecture with a MODE feature that can be used to operate the device in pulse-width modulation (PWM), pulse-frequency modulation (PFM), or discontinuous-conduction mode (DCM) control schemes. PWM operation provides constant frequency operation at all loads, and is useful in applications sensitive to switching frequency. PFM operation disables negative inductor current and additionally skips pulses at light loads for high efficiency. DCM features constant frequency operation down to lighter loads than PFM mode, by not skipping pulses but only disabling negative inductor current at light loads. DCM operation offers efficiency performance that lies between PWM and PFM modes. The low-resistance, on-chip MOSFETs ensure high efficiency at full load and simplify the layout. A programmable soft-start feature allows users to reduce input inrush current. The device also incorporates an output enable/undervoltage lockout pin (EN/UVLO) that allows the user to turn on the part at the desired input-voltage level. An open-drain active-low RESET pin provides a delayed power-good signal to the system upon achieving successful regulation of the output voltage.

II. Manufacturing Information

A. Description/Function:	4.5V-60V, 2.5A, High-Efficiency, Synchronous Step-Down DC-DC Converter with Internal Compensation
B. Process:	S18
C. Number of Device Transistors:	22048
D. Fabrication Location:	USA
E. Assembly Location:	Taiwan
F. Date of Initial Production:	September 18, 2013

III. Packaging Information

A. Package Type:	20-pin TQFN
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5249
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level1
J. Single Layer Theta Ja:	48°C/W
K. Single Layer Theta Jc:	2°C/W
L. Multi Layer Theta Ja:	33°C/W
M. Multi Layer Theta Jc:	2°C/W

IV. Die Information

A. Dimensions:	
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 77 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 14.3 \times 10^{-9}$

$\lambda = 14.3$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25°C and 0.93 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SANQ4Q001A, D/C 1326)

The PI02-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114.

Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78 With the following exceptions:

EN/UVLO pin passes +100mA/-30mA per JEDEC JESD78

Table 1

Reliability Evaluation Test Results

MAX17503ATP+T / MAX17504ATP+T / MAX17505ATP+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	77	0	SANQ4Q001D, D/C 1326

Note 1: Life Test Data may represent plastic DIP qualification lots.