MAX1748EUE
Rev. A

RELIABILITY REPORT

FOR

MAX1748EUE

PLASTIC ENCAPSULATED DEVICES

May 28, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX1748 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1748 triple-output DC-DC converter in a low-profile TSSOP package provides the regulated voltages required by active matrix, thin-film transistor (TFT) liquid crystal displays (LCDs). One high-power DC-DC converter and two low-power charge pumps convert the +3.3V to +5V input supply voltage into three independent output voltages.

The primary high-power DC-DC converter generates a boosted output voltage (V_{MAIN}) up to 13V that is regulated within ±1%. The low-power BiCMOS control circuitry and the low on-resistance (0.35 ohm) of the integrated power MOSFET allows efficiency up to 93%. The 1MHz current-mode PWM architecture provides fast transient response and allows the use of ultra-small inductors and ceramic capacitors.

The dual charge pumps independently regulate one positive output (V_{POS}) and one negative output (V_{NEG}). These low-power outputs use external diode and capacitor stages (as many stages as required) to regulate output voltages up to +40V and down to -40V. A proprietary regulation algorithm minimizes output ripple, as well as capacitor sizes for both charge pumps.

The MAX1748 is available in the ultra-thin TSSOP package (1.1mm max height).

B. Absolute Maximum Ratings

Item	Rating
IN,/SHDN,TGND to GND	-0.3V to +6V
DRVN to GND	-0.3V to (VSUPN + 0.3V)
DRVP to GND	-0.3V to (VSUPN + 0.3V)
PGND to GND	+/-0.3V
/RDY to GND	-0.3V to +14V
LX, SUPP, SUPN to PGND	-0.3V to +14V
INTG, REF,FB,FBN,FBP TO GND	-0.3V TO (VIN +0.3V)
Junction Temperature	+150°C
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
16-Pin TSSOP	755mW
Derates above +70°C	
16-Pin TSSOP	9.4mW/°C

II. Manufacturing Information

A. Description/Function:	Triple-Output TFT LCD DC=DC Converter
B. Process:	S8 - Standard .8 micron silicon gate CMOS
C. Number of Device Transistors:	2846
D. Fabrication Location:	California, USA
E. Assembly Location:	Thailand or Philippines
F. Date of Initial Production:	July, 2000

III. Packaging Information

A. Package Type:	**16-Lead TSSOP**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1101-0147
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	83 x 93 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Si
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 160 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 6.79 \times 10^{-9}$ λ = 6.79 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5523) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PX78 die type has been found to have all pins able to withstand a transient pulse of ±500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX1748EUE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	160	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	140	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Process/Package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

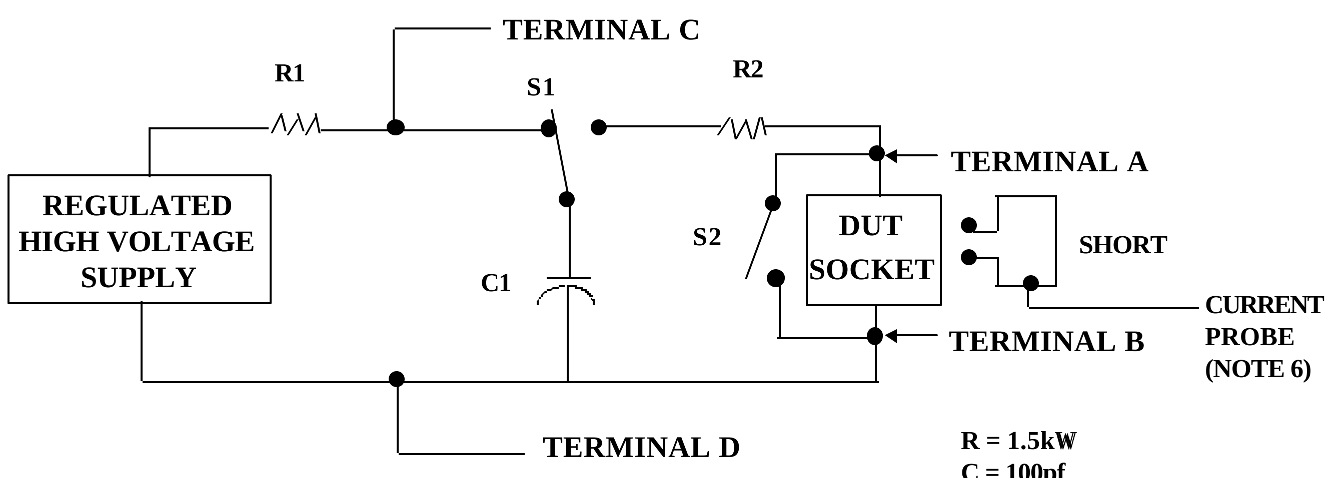
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_{S,}$ $-V_{S}$, V_{REF}, etc).

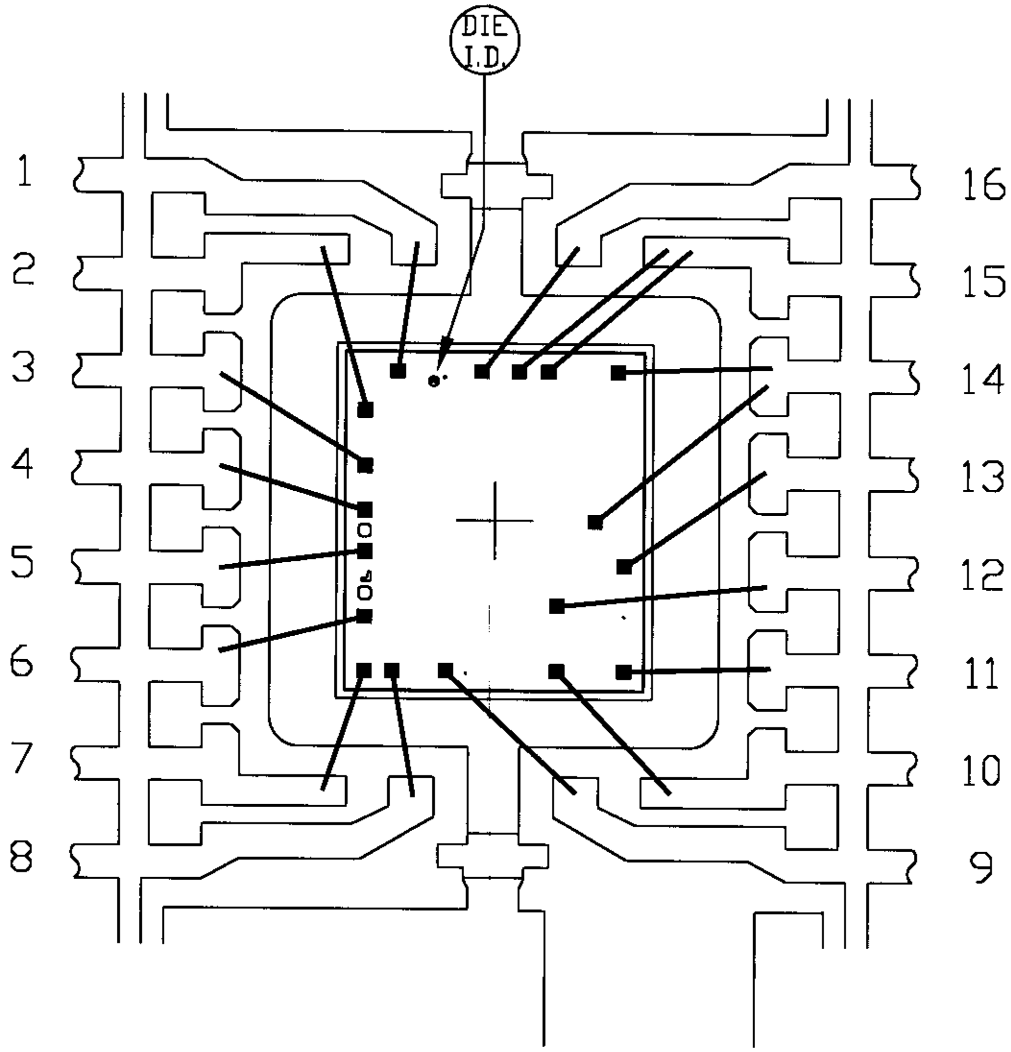
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

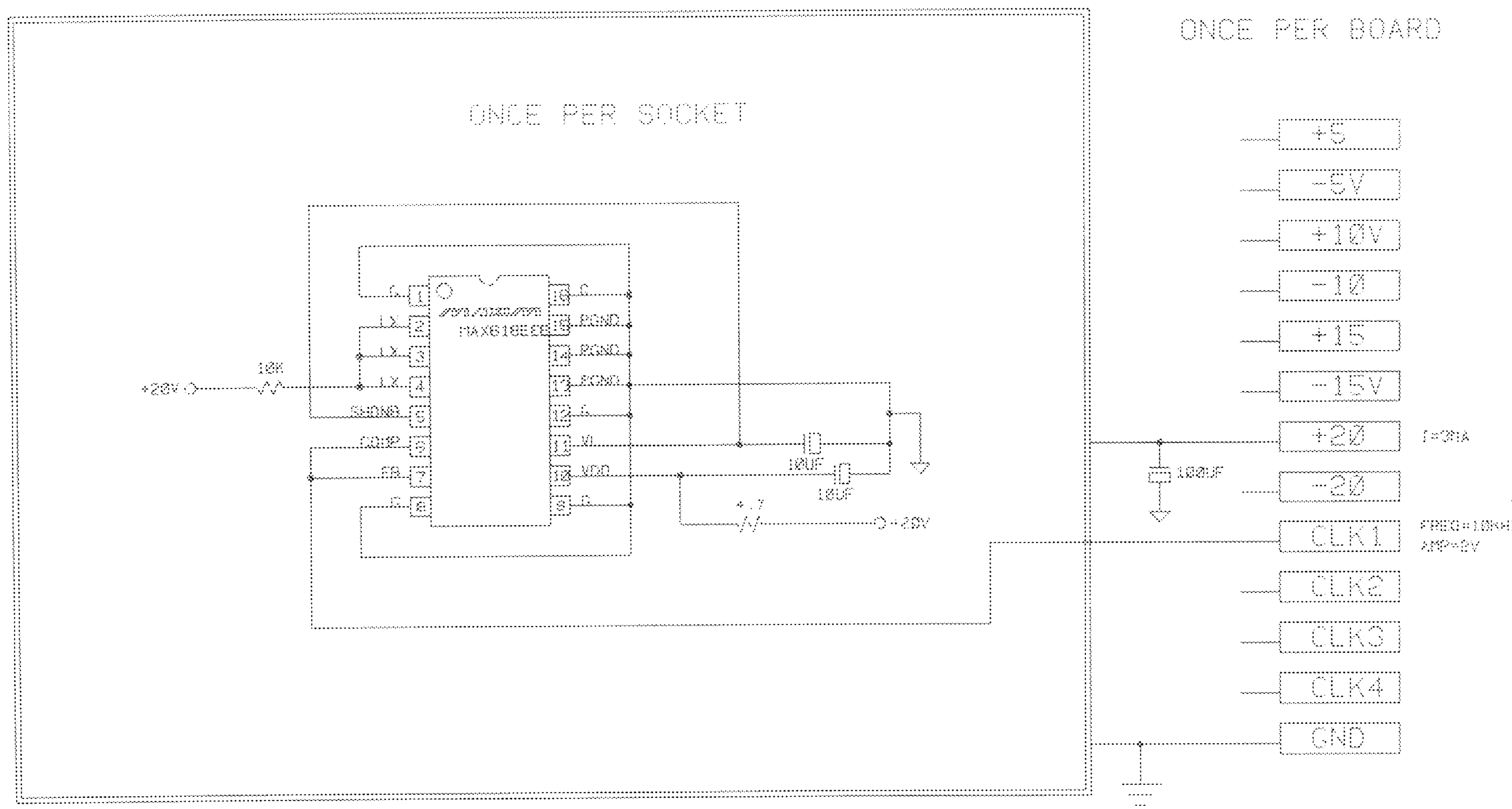
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE: U16-2		APPROVALS	DATE		
CAV./PAD SIZE: 118X118	PKG. DESIGN			BUILDSHEET NUMBER: 05-1101-0147	REV.: A



__ Steady state life test is per MIL-STD-883 Method 1005.
__ Burn-in is per MIL-STD-883 Method 1015. Cond. B

NOTES:

1. Temperature: +125oC or equivalent
2. Time: 160 hours min. or equivalent
3. All components and material must stand +150oC continuous
4. Approved for [ ] Commercial
   [ ] HR/883

MAXIM	CREATED: 08/15/95	BY: JH	ENG1:		ENG2: --	
	LAST SAVED: 16:26:13 02-24-99		SIZE B	A REVISION 00/00/00	DWG NO. --	
MAX618EEE	PROJECT: PX29					
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