RELIABILITY REPORT

FOR

MAX1692EUB

PLASTIC ENCAPSULATED DEVICES

February 14, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX1692 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1692 is a low-noise, pulse-width-modulated (PWM), DC-DC step-down converter. It powers logic and transmitters in small wireless systems such as cellular phones, communicating PDAs, and handy-terminals. The device features an internal synchronous rectifier for high efficiency; it requires no external Schottky diode. Excellent noise characteristics and fixed-frequency operation provide easy post-filtering. The MAX1692 is ideally suited for Li-Ion battery applications. It is also useful for +3V or +5V fixed input applications.

The device operates in one of four modes. Forced PWM mode operates at a fixed frequency regardless of the load. Synchronizable PWM mode allows an external switching frequency to control and minimize harmonics. Idle Mode™ (PWM/PFM) extends battery life by switching to a PFM pulse-skipping mode during light loads. Shutdown mode places the device in standby, reducing quiescent supply current to under 0.1µA.

The MAX1692 can deliver over 600mA. The output voltage can be adjusted from 1.25V to VIN with the input range of +2.7V to +5.5V. Other features of the MAX1692 include high efficiency, low dropout voltage, and a 1.2%-accurate 1.25V reference. It is available in a space-saving 10-pin µMAX package with a height of only 1.11mm.
The MAX6021 precision, low-dropout, micropower voltage reference is available in miniature SOT23-3 surface-mount package. It features a proprietary curvature-correction circuit and laser-trimmed thin-film resistors that result in a low temperature coefficient of <15ppm/°C and initial accuracy of better than 0.2%. This device is specified over the extended temperature range.

B. Absolute Maximum Ratings

Item	Rating
IN, BP, SHDN, SYNC/PWM, LIM to GND	-0.3V to +6V
BP to IN	-0.3V to +0.3V
PGND to GND	-0.3V to +0.3V
LX to PGND	-0.3V to (VIN + 0.3V)
FB, REF to GND	-0.3V to (VBP + 0.3V)
Reference Current	±1mA
LX Peak Current (internally limited)	1.6A
Continuous Power Dissipation (TA = +70°C)	
10-Pin µMAX (derate 5.6mW/°C above +70°C)	444mW
Operating Temperature Range	-40°C to +85°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10sec)	+300°C
Continuous Power Dissipation (TA = +70°C)	
10-Pin uMAX	444mW
Derates above +70°C	
10-Pin uMAX	5.6mW/°C

II. Manufacturing Information

A. Description/Function:	Low-Noise, 5.5V-Input, PWM Step-Down Regulator
B. Process:	S12 (Standard 1.2 micron silicon gate CMOS)
C. Number of Device Transistors:	1462
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia, Thailand or Philippines
F. Date of Initial Production:	July, 1998

III. Packaging Information

A. Package Type:	**10-Pin uMAX**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05- 1101-0094
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1

IV. Die Information

A. Dimensions:	87 x 61mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°Cbiased (static) life test are shown in **Table 1** Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.57 \times 10^{-9}$

$\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5349) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PX41 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX1692EUB

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	uMAX	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

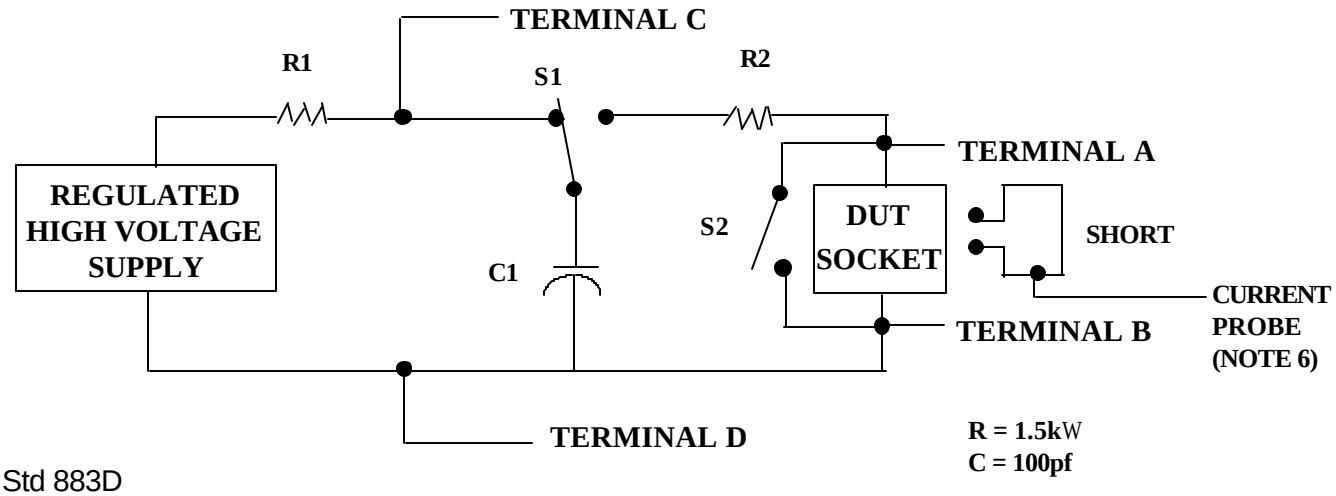
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

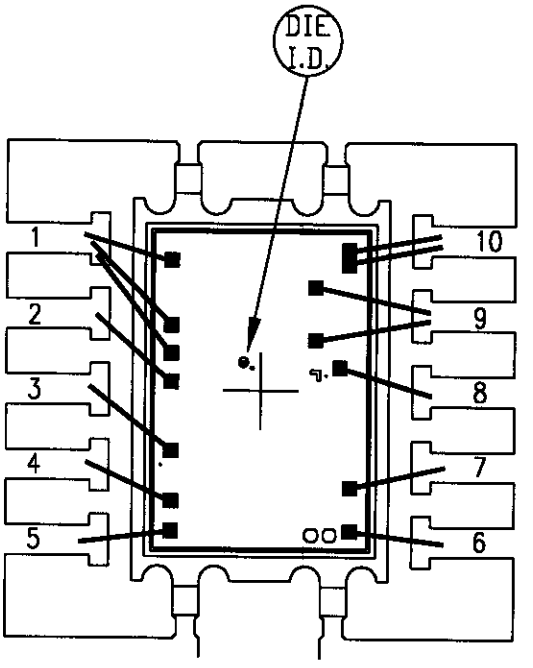
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

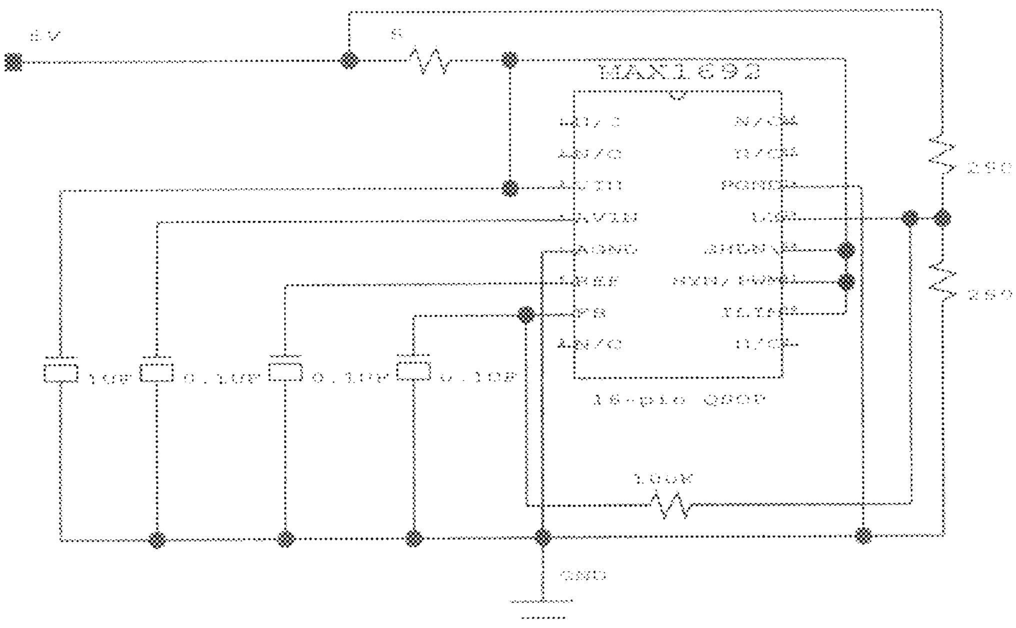
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8



PKG.CODE: U10-2		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 68X94	PKG. DESIGN			BUILDSHEET NUMBER: 05-1101-0094 / REV.: A



MAXIM CONFIDENTIAL

CREATED: 12/19/97 BY: LH

LAST SAVED: 6-2-1998_12:03

PX41BI

PROJECT: PX41

DESC.: BURN-IN CIRCUIT

SIZE A

A REVISION 00/00/00

DWG NO. —

FILE: PX41BI

SHEET 1 OF 1