RELIABILITY REPORT

FOR

MAX1659ESA+

PLASTIC ENCAPSULATED DEVICES

April 9, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX1659ESA+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX1658/MAX1659 linear regulators maximize battery life by combining ultra-low supply currents and low dropout voltages. They feature Dual Mode™ operation, which presets the output to 3.3V (MAX1658) or 5V (MAX1659), or permits it to be adjusted between 1.25V and 16V. The regulator supplies up to 350mA, with a typical dropout of 650mV for the MAX1658 and 490mV for the MAX1659. With their p-channel MOSFET pass transistor, these devices maintain a low quiescent current from zero output current to the full 350mA, even in dropout. They support input voltages ranging from 2.7V to 16.5V. The MAX1658/MAX1659 feature a 1µA shutdown mode, reverse battery protection, short-circuit protection, and thermal shutdown. They are available in a special high-power (1.2W), 8-pin SO package designed specifically for compact applications.

II. Manufacturing Information

A. Description/Function:	350mA, 16.5V Input, Low-Dropout Linear Regulators
B. Process:	SG5
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Thailand
F. Date of Initial Production:	July 26, 1997

III. Packaging Information

A. Package Type:	8-pin SOIC (N)
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (2 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-1701-0326
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	102.7°C/W
K. Single Layer Theta Jc:	32°C/W
L. Multi Layer Theta Ja:	77°C/W
M. Multi Layer Theta Jc:	32°C/W

IV. Die Information

A. Dimensions:	89X132 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	5.0 microns (as drawn)
F. Minimum Metal Spacing:	5.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 320 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 7.58 \times 10^{-9}$

$\lambda = 7.58$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the SG5 Process results in a FIT Rate of 0.11 @ 25C and 1.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot NVEBD4008A, D/C 0005)

The PW97-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1

Reliability Evaluation Test Results

MAX1659ESA+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	160	1	NVEAD4008A, D/C 0005
	Biased	& functionality	80	0	NVEACV001A, D/C 9908
	Time = 192 hrs.		80	0	XVEABB001A, D/C 9727

Note 1: Life Test Data may represent plastic DIP qualification lots.