RELIABILITY REPORT

FOR

MAX1634xAI

PLASTIC ENCAPSULATED DEVICES

August 23, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Manager, Reliability Operations

Conclusion

The MAX1634 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1634 is a buck-topology, step-down, switch-mode, power-supply controller that generates logic-supply voltages in battery-powered systems. This high-performance, dual/triple-output device includes on-board power-up sequencing, power-good signaling with delay, digital soft-start, secondary winding control, low-dropout circuitry, internal frequency-compensation networks, and automatic bootstrapping.

Up to 96% efficiency is achieved through synchronous rectification and Maxim's proprietary Idle Mode™ control scheme. Efficiency is greater than 80% over a 1000:1 load-current range, which extends battery life in system-suspend or standby mode. Excellent dynamic response corrects output load transients caused by the latest dynamic-clock CPUs within five 300kHz clock cycles. Strong 1A on-board gate drivers ensure fast external N-channel MOSFET switching.

This device features a logic-controlled and synchronizable, fixed-frequency, pulse-width-modulation (PWM) operating mode. This reduces noise and RF interference in sensitive mobile communications and pen-entry applications. Asserting the SKIP-bar pin enables fixed-frequency mode, for lowest noise under all load conditions.

The MAX1634 includes two PWM regulators, adjustable from 2.5V to 5.5V with fixed 5.0V and 3.3V modes. This device includes secondary feedback regulation. The MAX1634 includes a secondary feedback input (SECFB), plus a control pin (STEER) that selects which PWM (3.3V or 5V) receives the secondary feedback signal. SECFB provides a method for adjusting the secondary winding voltage regulation point with an external resistor divider, and is intended to aid in creating auxiliary voltages other than fixed 12V.

B. Absolute Maximum Ratings

Item	Rating
V+ to GND	-0.3V to +36V
PGND to GND	±0.3V
VL to GND	-0.3V to +6V
BST3, BST5 to GND	-0.3V to +36V
LX3 to BST3	-6V to +0.3V
LX5 to BST5	-6V to +0.3V
REF, SYNC, SEQ, STEER, SKIP, TIME/ON5, SECFB, RESET to GND	-0.3V to +6V
VDD to GND	-0.3V to +20V
RUN/ON3, SHDN to GND	-0.3V to (V+ + 0.3V)
12OUT to GND	-0.3V to (VDD + 0.3V)
DL3, DL5 to PGND	-0.3V to (VL + 0.3V)
DH3 to LX3	-0.3V to (BST3 + 0.3V)
DH5 to LX5	-0.3V to (BST5 + 0.3V)
VL, REF Short to GND	Momentary
12OUT Short to GND	Continuous
REF Current	+5mA to -1mA
VL Current	+50mA
12OUT Current	+200mA
VDD Shunt Current	+15mA
Operating Temperature Ranges	
MAX1634CAI	0°C to +70°C
MAX1634EAI	-40°C to +85°C
Storage Temperature Range	-65°C to +160°C
Continuous Power Dissipation (TA = +70°C)	
SSOP (derate 9.52mW/°C above +70°C)	762mW
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function: Multi-Output, Low-Noise Power-Supply Controllers for Notebook Computers

B. Process: B12 (Standard 1.2 micron silicon gate CMOS)

C. Number of Device Transistors: 4886

D. Fabrication Location: California or Texas, USA

E. Assembly Location: Malaysia or Philippines

F. Date of Initial Production: Febuary, 1997

III. Packaging Information

A. Package Type: **28-Pin SSOP**

B. Lead Frame: Copper

C. Lead Finish: 100% Matte Tin

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: # 05-1701-0238

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C: Level 1

IV. Die Information

A. Dimensions: 92 x 128 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 1.2 microns (as drawn)

F. Minimum Metal Spacing: 1.2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA**)**

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 491 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 2.24 \times 10^{-9}$

λ = 2.24 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Attached Burn-In Schematic (Spec. # 06-5116B) shows the static Burn-In circuit. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the B8/S8 Process results in a FIT rate of 0.10 @ 25°C and 1.78 @ 55°C (eV = 0.8, UCL = 60%).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PW57R-4 die type has been found to have all pins able to withstand a transient pulse of ±400V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX1634xAI

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		491	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	28 Pin SSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

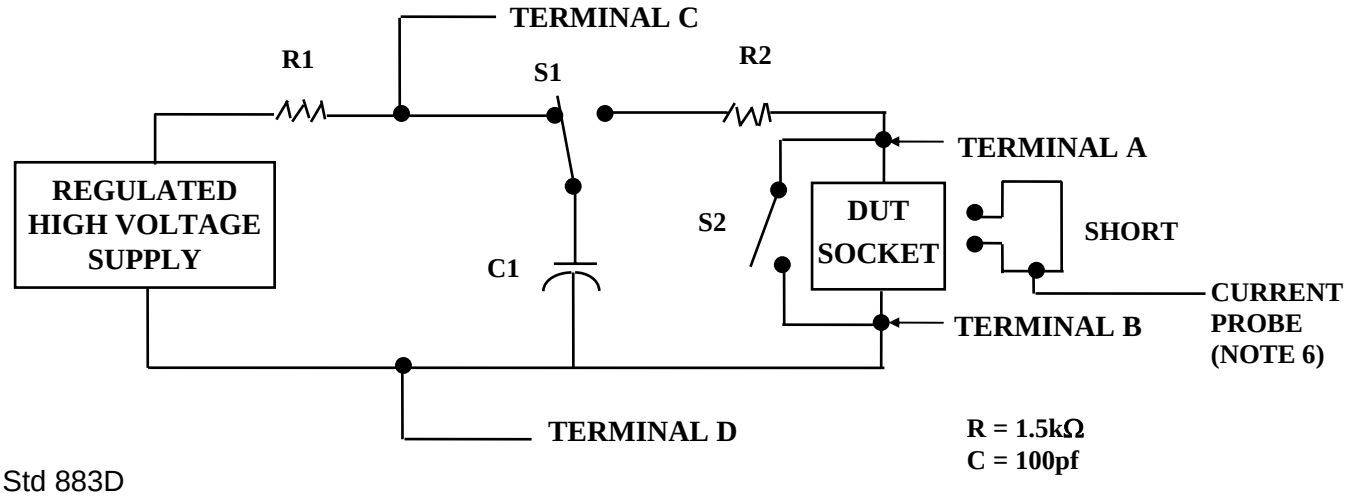
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

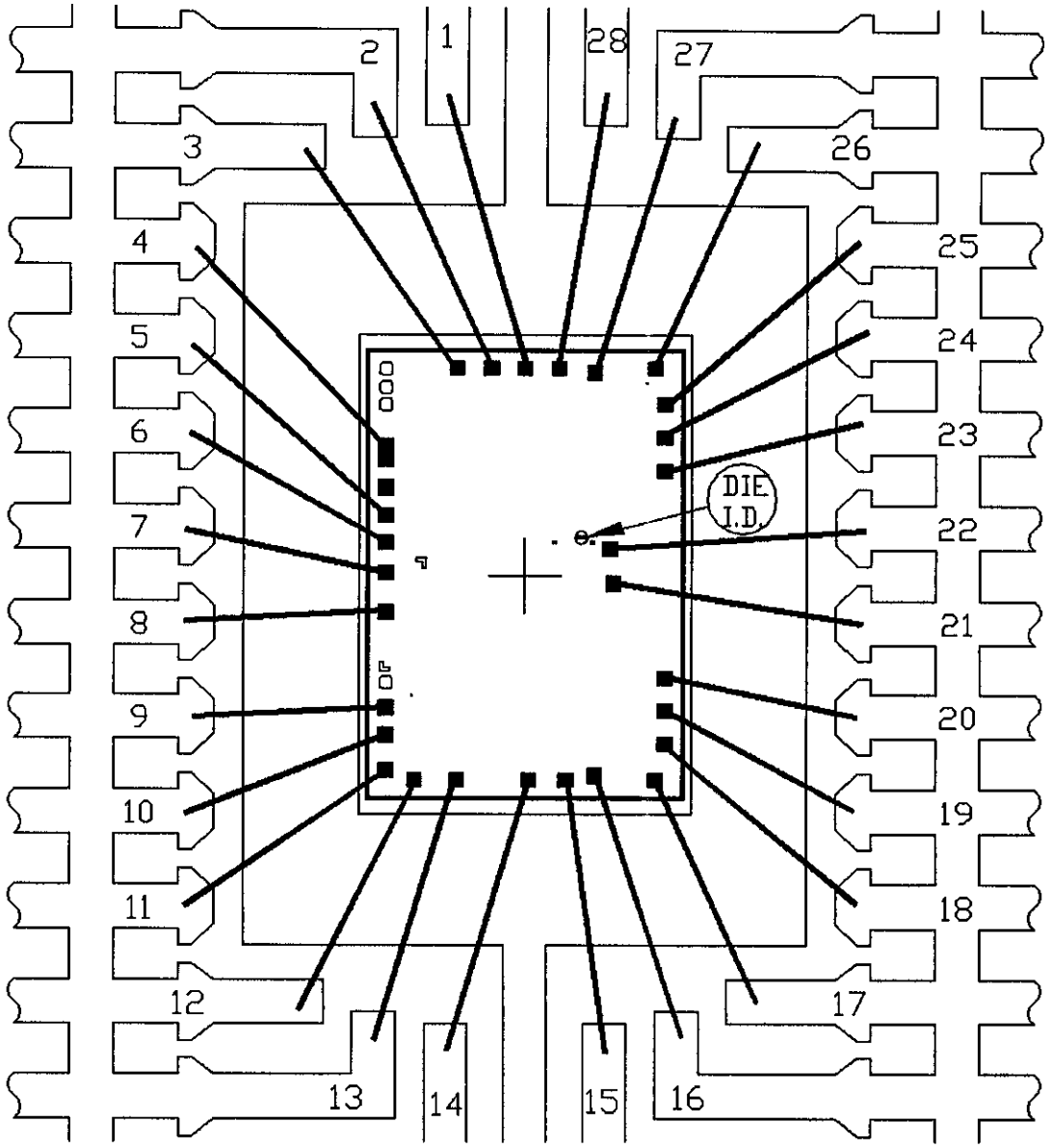
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

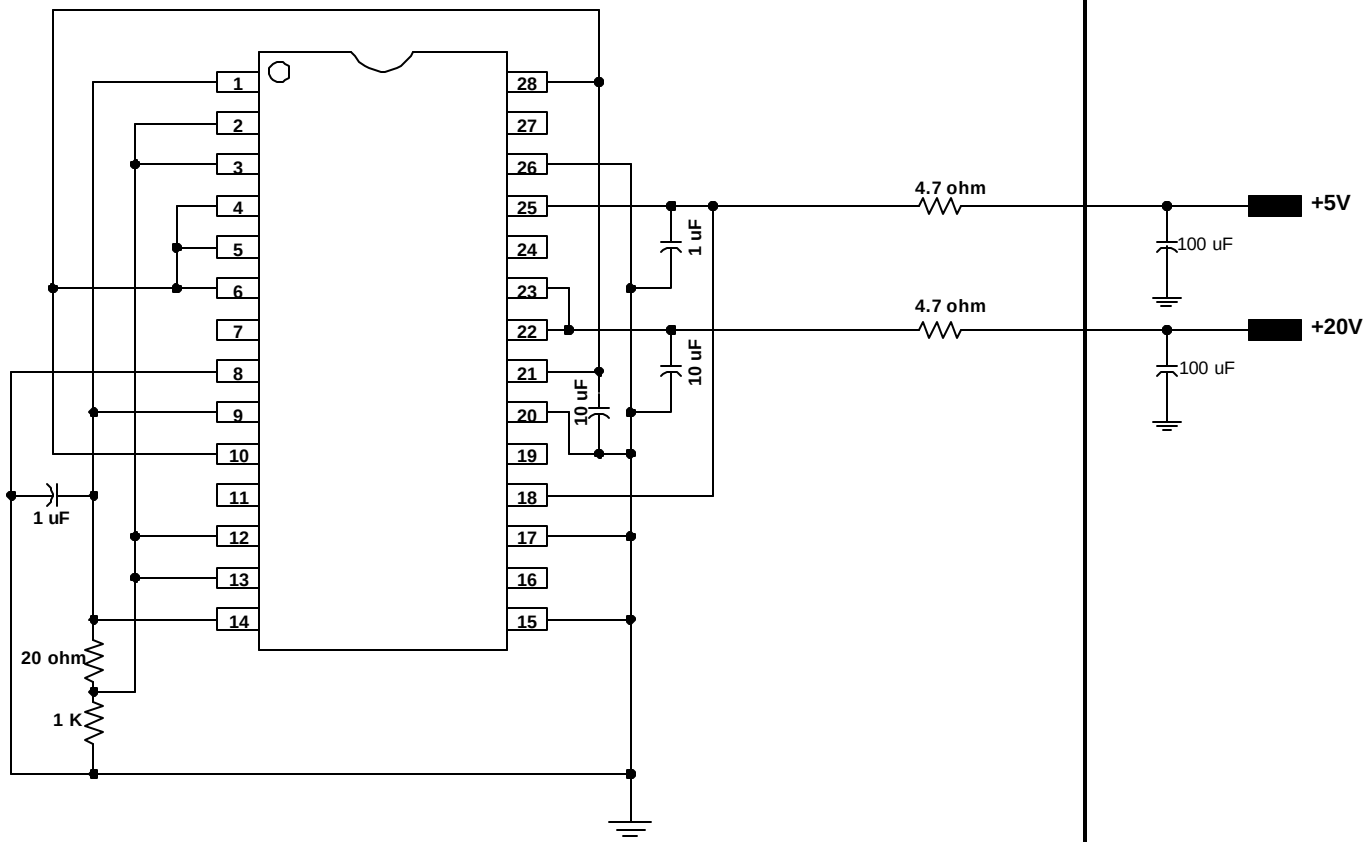




PKG.CODE: A28-1		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 154X200	PKG. DESIGN			BUILDSHEET NUMBER: 05-1701-0238 / REV.: A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 1631/1634/1901/1904
PACKAGE= 28-SSOP
MAX. EXPECTED CURRENT = 5mA

NOTES: