RELIABILITY REPORT

FOR

MAX1620EEE+T

PLASTIC ENCAPSULATED DEVICES

July 25, 2012

MAXIM INTEGRATED PRODUCTS

160 Rio Robles

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Approved by
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Conclusion

The MAX1620EEE+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1620/MAX1621 convert a 1.8V to 20V battery voltage to a positive or negative LCD backplane bias voltage. Backplane bias voltage can be automatically disabled when the display logic voltage is removed, protecting the display. These devices use very little PC board area, come in ultra-small QSOP packages, and require only small, low-profile external components. Output voltage can be set to a desired positive or negative voltage range with external resistors, and adjusted over that range with the on-board digital-to-analog converter (DAC) or with a potentiometer. The MAX1620/ MAX1621 include a 5-bit DAC, allowing digital software control of the bias voltage. The MAX1620 uses up/down digital signaling to adjust the DAC, and the MAX1621 uses the System Management Bus (SMBus(tm)) 2-wire serial interface. These devices use a low-cost, external, N-channel MOSFET power switch or NPN transistor, and can be configured for positive or negative output voltages. Operating current is a low 150µA, typically provided from a display's logic supply of 3.0V to 5.5V. The MAX1620/MAX1621 are available in a 16-pin QSOP package.

II. Manufacturing Information

A. Description/Function:	Digitally Adjustable LCD Bias Supplies
B. Process:	S12
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Malaysia, Philippines, Thailand
F. Date of Initial Production:	July 26, 1997

III. Packaging Information

A. Package Type:	0.150 16L QSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-1701-0314 / A
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	120°C/W
K. Single Layer Theta Jc:	37°C/W
L. Multi Layer Theta Ja:	103.7°C/W
M. Multi Layer Theta Jc:	37°C/W

IV. Die Information

A. Dimensions:	58 X 81 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{4.04}{192 \times 4340 \times 280 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 8.7 \times 10^{-9}$

$\lambda = 8.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S12 Process results in a FIT Rate of 0.17 @ 25C and 3.00 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot NINAGX002A D/C 9750)

The PW55 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX1620EEE+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	80	0	NINAGX002A, D/C 9750
	Biased	& functionality	80	1	BINAEX002C, D/C 9726
	Time = 192 hrs.		80	0	BINBDS002C, D/C 9706
			40	0	BINADX002A, D/C 9706

Note 1: Life Test Data may represent plastic DIP qualification lots.