## RELIABILITY REPORT

FOR

# MAX1614EUA

PLASTIC ENCAPSULATED DEVICES

June 20, 2003

# **MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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#### Conclusion

The MAX1614 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX1614 drives high-side, N-channel power MOSFETs to provide battery power-switching functions in portable equipment. N-channel power MOSFETs typically have one-third the on-resistance of P-channel MOSFETs of similar size and cost. An internal micropower regulator and charge pump generate the high-side drive output voltage, while requiring no external components.

The MAX1614 also features a 1.5%-accurate low-battery comparator that can be used to indicate a low-battery condition, provide an early power-fail warning to the system microprocessor, or disconnect the battery from the load, preventing deep discharge and battery damage. An internal latch allows for pushbutton on/off control with very low current consumption. Off-mode current consumption is only  $6\mu$ A while normal operation requires less than  $25\mu$ A. The MAX1614 is available in the space-saving  $\mu$ MAX package that occupies about 60% less space than a standard 8-pin SO.

Doting

# B. Absolute Maximum Ratings

<u>item</u>	Rating
BATT, SRC to GND	-0.3V to +30V
GATE to SRC	-0.3V to +12V
GATE to GND	-0.3V to +36V
GATE + SRC Sink Current, Continuous	2.7mA
LBI, LBO, ON, OFF to GND	-0.3V to +12V
LBO Current	5mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10sec)	+300°C
Continuous Power Dissipation (TA = +70°C)	
8-Pin μMAX	330mW
Derates above +70°C	
8-Pin μMAX	4.1mW/°C

## **II.** Manufacturing Information

A. Description/Function: High-Side, N-Channel MOSFET Switch Driver

B. Process: S3 (Standard 3 micron silicon gate CMOS)

C. Number of Device Transistors: 264

D. Fabrication Location: Oregon, USA

Philippines, Korea or Thailand E. Assembly Location:

F. Date of Initial Production: March, 1997

## III. Packaging Information

A. Package Type: 8-Pin µMAX

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: #05-1101-0005

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity

per JEDEC standard JESD22-112: Level 1

## IV. Die Information

A. Dimensions: 58 x 84 mils

B. Passivation: Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub> (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 3 microns (as drawn)

F. Minimum Metal Spacing: 3 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO<sub>2</sub>

Wafer Saw I. Die Separation Method:

## V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations)

Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

#### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \underbrace{\frac{1}{\text{MTTF}}}_{\text{F}} = \underbrace{\frac{1.83}{192 \text{ x } 4389 \text{ x } 160 \text{ x } 2}}_{\text{Temperature Acceleration factor assuming an activation energy of } \text{Chi square value for MTTF upper limit)}$$

$$\lambda = 6.79 \times 10^{-9}$$

 $\lambda$  = 6.79 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5229) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (RR-1M).

#### B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard  $85^{\circ}$ C/85%RH testing is done per generic device/package family once a quarter.

#### C. E.S.D. and Latch-Up Testing

The PX01 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2000$ V per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250$ mA.

# Table 1 Reliability Evaluation Test Results

# MAX1614EUA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	t (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		160	0
Moisture Testir	ng (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	uMAX	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Str	ess (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots. Note 2: Generic Package/Process data

#### Attachment #1

TABLE II. Pin combination to be tested. 1/2/

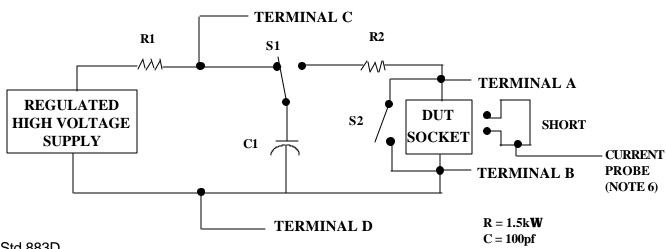
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V <sub>PS1</sub> 3/	All V <sub>PS1</sub> pins
2.	All input and output pins	All other input-output pins

- 1/ Table II is restated in narrative form in 3.4 below.
- 2/ No connects are not to be tested.
- 3/ Repeat pin combination I for each named Power supply and for ground

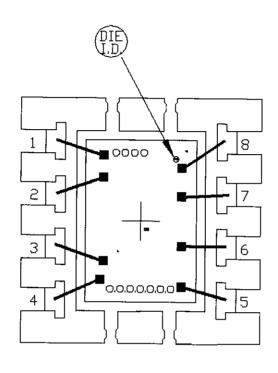
(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_{S}$ ,  $-V_{S}$ ,  $V_{REF}$ , etc).

# 3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., \( \lambda\_{S1} \), or \( \lambda\_{S2} \) or \( \lambda\_{S3} \) or \( \lambda\_{CC1} \), or \( \lambda\_{CC2} \)) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D Method 3015.7 Notice 8



PKG.CDDE: U8-1		APPROVALS	DATE
CAV./PAD SIZE: 68X94	PKG. DESIGN		<b>.</b>



