RELIABILITY REPORT

FOR

MAX16072RS29D2+T

WAFER LEVEL DEVICES

March 8, 2017

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Eric Wright Reliability Engineer	Brian Standley Manager, Reliability

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Conclusion

The MAX16072RS29D2+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX16072/MAX16073/MAX16074 ultra-small, ultra-low-power, microprocessor (µP) supervisory circuits feature a precision band-gap reference, comparator, and internally trimmed resistors that set the threshold voltage. Designed to monitor the system supply voltage and assert an output during power-up, power-down, and brownout conditions, these devices provide excellent circuit reliability and low cost by eliminating external components and adjustments when monitoring nominal system voltage from 1.8V to 3.6V. The MAX16072 has a push-pull, active-low reset output, the MAX16073 has a push-pull, active-high reset output, and the MAX16074 has an open-drain active-low reset output. The devices are designed to ignore fast transients on VCC. The devices also include a manual reset input (active-low MR). The MAX16072/MAX16073/MAX16074 are available in a 1mm x 1mm, space-saving, 4-bump, chip-scale package (UCSP(tm)).

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II. Manufacturing Information

A. Description/Function:	µP Supervisory Circuits in 4-Bump (1mm x 1mm) Chip-Scale Package
B. Process:	B8
C. Number of Device Transistors:	526
D. Fabrication Location:	USA
E. Assembly Location:	Thailand
F. Date of Initial Production:	January 18, 2010

III. Packaging Information

A. Package Type:	4-bump UCSP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	None
G. Assembly Diagram:	#05-9000-3935
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A°C/W
K. Single Layer Theta Jc:	N/A°C/W
L. Multi Layer Theta Ja:	335°C/W
M. Multi Layer Theta Jc:	N/A°C/W

IV. Die Information

A. Dimensions:	45X45 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Isolation Dielectric:	SiO_2
H. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Eric Wright (Reliability Engineering)
Brian Standley (Manager, Reliability)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

λ = 22.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the B8 Process results in a FIT Rate of 0.06 @ 25C and 0.99 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The MT18 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

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Table 1

Reliability Evaluation Test Results

MAX16072RS29D2+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.

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