RELIABILITY REPORT

FOR

MAX1589AEZTxxx+T / MAX1589AETTxxx+T

PLASTIC ENCAPSULATED DEVICES

July 7, 2011

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

| **Approved by** |
|---|
| Richard Aburano |
| Quality Assurance |
| Manager, Reliability Engineering |

**Conclusion**

The MAX1589AEZTxxx+T/MAX1589AETTxxx+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

**Table of Contents**



**I. Device Description**

A. General

The MAX1589A low-dropout linear regulator operates from a +1.62V to +3.6V supply and delivers a guaranteed 500mA continuous load current with a low 175mV dropout. The high-accuracy (±0.5%) output voltage is preset to internally trimmed voltages from +0.75V to +3.0V. An active-low, open-drain reset output remains asserted for at least 70ms after the output voltage reaches regulation. This device is offered in 6-pin thin SOT23 and 6-pin, 3mm x 3mm thin DFN packages.

An internal pMOS pass transistor maintains low supply current, independent of load and dropout voltage, making the MAX1589A ideal for portable battery-powered equipment such as personal digital assistants (PDAs), digital still cameras, cell phones, cordless phones, and notebook computers. Other features include logic-controlled shutdown, short-circuit protection, and thermal-overload protection.

**II. Manufacturing Information**

| | | |
|---|---|---|
| A. Description/Function: | Low-Input-Voltage, 500mA LDO Regulator with Active-Low RESET in SOT and TDFN | |
| B. Process: | S4 | |
| C. Number of Device Transistors: | | |
| D. Fabrication Location: | California, Texas or Japan | |
| E. Assembly Location: | Malaysia, Philippines and Thailand | Taiwan and Thailand |
| F. Date of Initial Production: | 2005 | |

**III. Packaging Information**

| | | |
|---|---|---|
| A. Package Type: | 6-pin TSOT | 6-pin TDFN 3x3 |
| B. Lead Frame: | Copper | Copper |
| C. Lead Finish: | 100% matte Tin | 100% matte Tin |
| D. Die Attach: | Conductive | Conductive |
| E. Bondwire: | Au (1 mil dia.) | Au (1 mil dia.) |
| F. Mold Material: | Epoxy with silica filler | Epoxy with silica filler |
| G. Assembly Diagram: | #05-9000-0802 | #05-9000-0804 |
| H. Flammability Rating: | Class UL94-V0 | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1 | Level 1 |
| J. Single Layer Theta Ja: | 365.1°C/W | 55°C/W |
| K. Single Layer Theta Jc: | 75°C/W | 9°C/W |
| L. Multi Layer Theta Ja: | 110°C/W | 42°C/W |
| M. Multi Layer Theta Jc: | 50°C/W | 9°C/W |

**IV. Die Information**

| | |
|---|---|
| A. Dimensions: | 50 X 36 mils |
| B. Passivation: | $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Al with Ti/TiN Barrier |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn) |
| F. Minimum Metal Spacing: | Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn) |
| G. Bondpad Dimensions: | |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

## V. Quality Assurance Information

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|---|---|
| A. Quality Assurance Contacts: | Richard Aburano (Manager, Reliability Engineering)<br>Don Lipps (Manager, Reliability Engineering)<br>Bryan Preeshl (Vice President of QA) |
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet.<br>0.1% For all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm |
| D. Sampling Plan: | Mil-Std-105D |

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 282 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 3.9 \times 10^{-9}$

$\lambda = 3.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S4 Process results in a FIT Rate of 0.05 @ 25C and 0.83 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SM20FA014B, D/C 0513)

The PM35 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 1500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of 250mA.

**Table 1**

Reliability Evaluation Test Results

**MAX1589AEZTxxx+T/MAX1589AETTxxx+T**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES | COMMENTS |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | | |
| | Ta = 135°C | DC Parameters | 79 | 0 | TM20G2125D, D/C 0806 |
| | Biased | & functionality | 79 | 0 | TM20G2060G, D/C 0802 |
| | Time = 192 hrs. | | 77 | 0 | SM20E2016B, D/C 0516 |
| | | | 47 | 0 | SM20E2016E, D/C 0515 |

Note 1: Life Test Data may represent plastic DIP qualification lots.