RELIABILITY REPORT

FOR

MAX1576ETG

PLASTIC ENCAPSULATED DEVICES

October 30, 2004

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Quality Assurance
Reliability Lab Manager

Conclusion

The MAX1576 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1576 charge pump drives up to 8 white LEDs with regulated constant current for uniform intensity. The main group of LEDs (LED1-LED4) can be driven up to 30mA per LED for backlighting. The flash group of LEDs (LED5-LED8) are independently controlled and can be driven up to 100mA per LED (or 400mA total). By utilizing adaptive 1x/1.5x/2x charge-pump modes and very-low-dropout current regulators, the MAX1576 achieves high efficiency over the full 1-cell lithium-battery voltage range. The 1MHz fixed-frequency switching allows for tiny external components, and the regulation scheme is optimized to ensure low EMI and low input ripple.

The MAX1576 uses two external resistors to set the main and flash full-scale (100%) LED currents. Four control pins are used for LED dimming by either serial control or 2-bit logic per group. ENM1 and ENM2 set the main LEDs to 10%, 30%, or 100% of full scale. ENF1 and ENF2 set the flash LEDs to 20%, 40%, or 100% of full scale. In addition, connect either pair of control pins together for single-wire, serial pulse dimming control.

The MAX1576 is available in a 24-pin thin QFN, 4mm x 4mm package (0.8mm max height).

B. Absolute Maximum Ratings

Item	Rating
INP, IN, OUT, ENM1, ENM2, ENF1, ENF2 to GND1	-0.3V to +6.0V
SETF, SETM, LED1, LED2, LED3, LED4, LED5, LED6, LED7, LED8 to GND1	-0.3V to (VIN + 0.3V)
C1N, C2N to GND1	-0.3V to (VIN + 1V)
C1P, C2P to GND1	-0.3V to Greater of (VOUT + 1V) or (VIN + 1V)
GND2, PGND to GND1	-0.3V to +0.3V
OUT Short Circuit to GND	Continuous
Continuous Power Dissipation (TA = +70°C)	
24-Pin 4mm x 4mm Thin QFN	1666mW
Derates above +70°C	
24-Pin 4mm x 4mm Thin QFN	20.8mW/°C

II. Manufacturing Information

A. Description/Function:	480mA White LED 1x/1.5x/2x Charge Pump for Backlighting and Camera Flash
B. Process:	B8 - Standard 8 micron silicon gate CMOS
C. Number of Device Transistors:	6679
D. Fabrication Location:	California, USA
E. Assembly Location:	Thailand or Hong Kong
F. Date of Initial Production:	July, 2004

III. Packaging Information

A. Package Type:	**24-Lead QFN (4x4)**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-9000-1122
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1

IV. Die Information

A. Dimensions:	100 X 100 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	TiW/ AlCu/ TiWN
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 22.62 \times 10^{-9}$ λ = 22.62 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-6345) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**) located on the Maxim website at http://www.maxim-ic.com .

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PN55 die type has been found to have all pins able to withstand a transient pulse of ±1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX1576ETG

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic process/package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

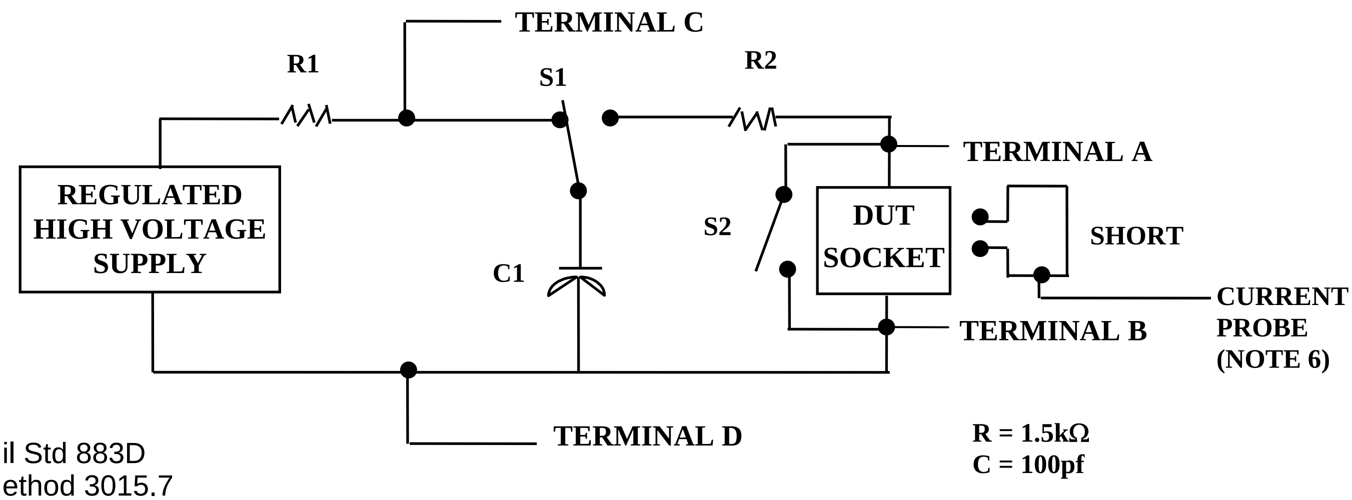
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_{S,}$ $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

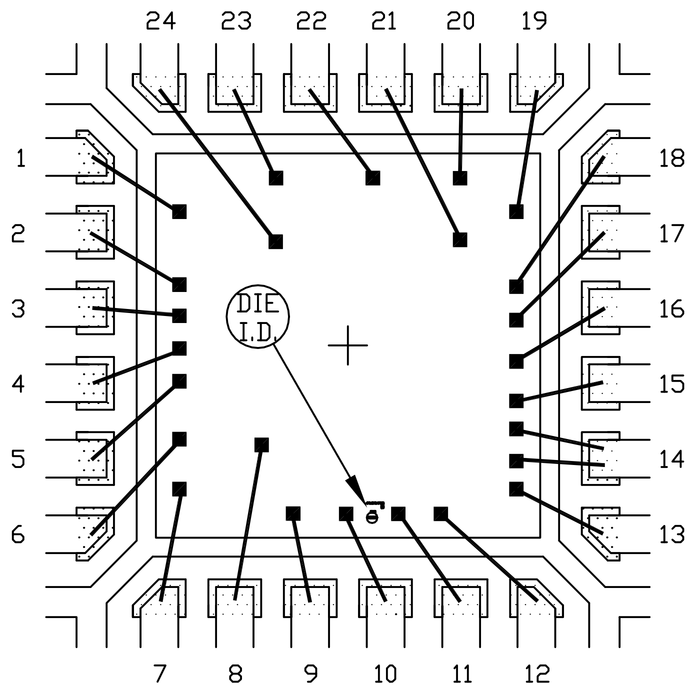
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



4x4x0.8mm THIN QFN PKG.

EXPOSED PAD PKG.

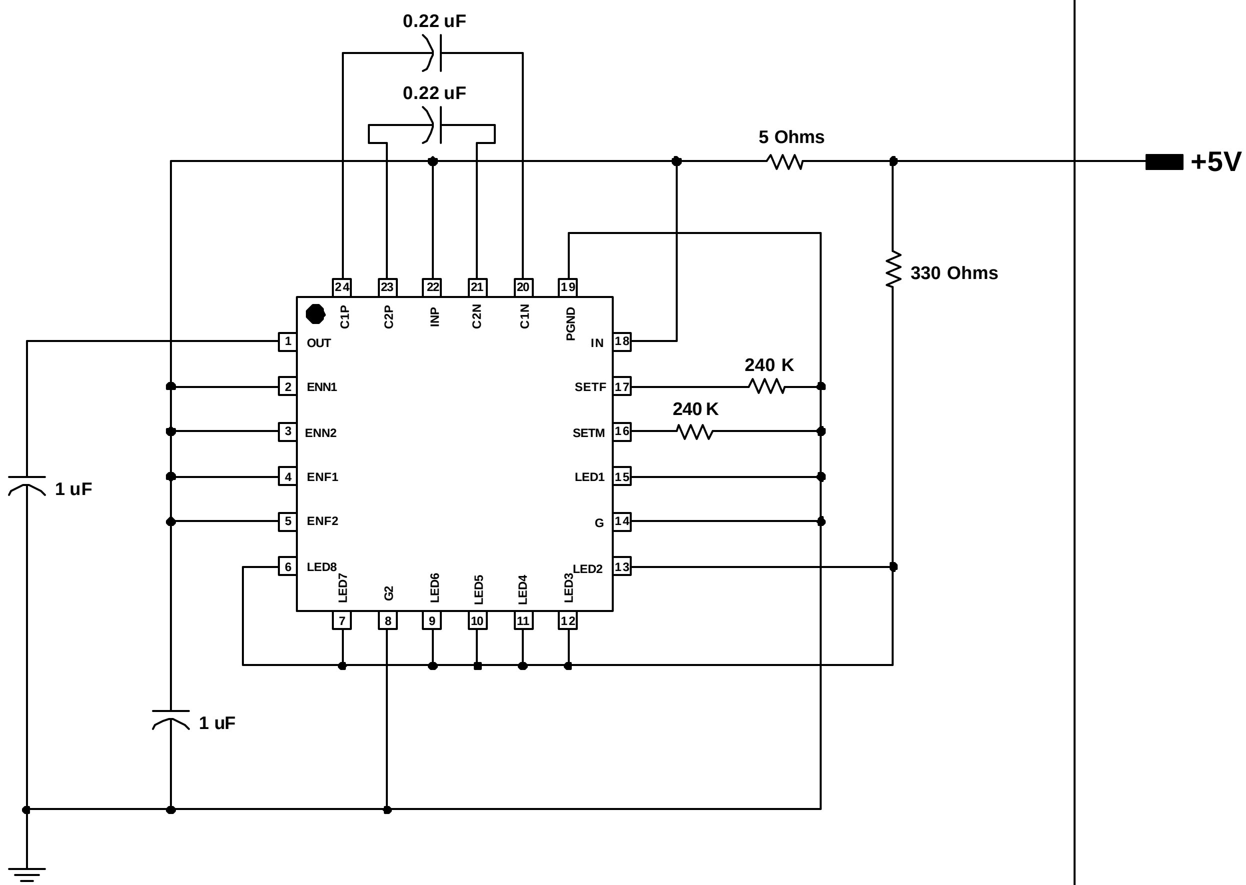


BONDABLE AREA

PKG. CODE: T2444-4		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 110x110	PKG.			BOND DIAGRAM #: 05-9000-1122	REV: B
	DESIGN				

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX1576 (PN55)
PACKAGE: 24-QFN 4x4 THIN
MAX EXPECTED CURRENT: 23mA, Typical : 20mA

NOTES:

DOCUMENT I.D. 06-6345	**REVISION** B	***MAXIM*** **TITLE: BI Circuit: MAX1576 (PN55)**	**PAGE** 2