RELIABILITY REPORT FOR

MAX15462AATA+T / MAX15462BATA+T / MAX15462CATA+T

PLASTIC ENCAPSULATED DEVICES

July 18, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Eric Wright
Quality Assurance
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Conclusion

The MAX15462AATA+T / MAX15462BATA+T / MAX15462CATA+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX15462 high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over a 4.5V to 42V input voltage range. The converter delivers output current up to 300mA at 3.3V (MAX15462A), 5V (MAX15462B), and adjustable output voltages (MAX15462C). The device operates over the -40°C to +125°C temperature range and is available in a compact 8-pin (2mm x 2mm) TDFN package. Simulation models are available. The device employs a peak-current-mode control architecture with a MODE pin that can be used to operate the device in the pulse-width modulation (PWM) or pulse-frequency modulation (PFM) control schemes. PWM operation provides constant frequency operation at all loads and is useful in applications sensitive to variable switching frequency. PFM operation disables negative inductor current and additionally skips pulses at light loads for high efficiency. The low-resistance on-chip MOSFETs ensure high efficiency at full load and simplify the PCB layout. To reduce input inrush current, the device offers an internal soft-start. The device also incorporates an EN/ UVLO pin that allows the user to turn on the part at the desired input-voltage level. An open-drain RESET pin can be used for output-voltage monitoring.

II. Manufacturing Information

A. Description/Function:	42V, 300mA, Ultra-Small, High-Efficiency, Synchronous Step-Down DC-DC Converters
B. Process:	S18
C. Number of Device Transistors:	17522
D. Fabrication Location:	USA
E. Assembly Location:	Thailand
F. Date of Initial Production:	March 27, 2015

III. Packaging Information

A. Package Type:	8-pin TDFN
B. Lead Frame:	Copper
C. Lead Finish:	NiPdAu
D. Die Attach:	Non-Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5241
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A°C/W
K. Single Layer Theta Jc:	N/A°C/W
L. Multi Layer Theta Ja:	162°C/W
M. Multi Layer Theta Jc:	20°C/W

IV. Die Information

A. Dimensions:	55.1181 X 65.3543 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25°C and 0.93 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The PI27-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX15462AATA+T / MAX15462BATA+T / MAX15462CATA+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	SAMR2Q001B, D/C 1320

Note 1: Life Test Data may represent plastic DIP qualification lots.