RELIABILITY REPORT

FOR

MAX15112EWG+T

WAFER LEVEL PRODUCTS

March 26, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX15112EWG+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX15112 high-efficiency, current-mode step-down regulator with integrated power switches operates from 2.7V to 5.5V and delivers up to 12A of output current in a small 2mm x 3mm package. The MAX15112 offers excellent efficiency with skip mode capability at light-load conditions, yet provides unmatched efficiency under heavy load conditions. The combination of small size and high efficiency makes this device suitable for both portable and nonportable applications. The MAX15112 utilizes a current-mode control architecture with a high-gain transconductance error amplifier, which allows a simple compensation scheme and enables a cycle-by-cycle current limit with fast response to line and load transients. A factory-trimmed switching frequency of 1MHz (PWM operation) allows for a compact, all-ceramic capacitor design. Integrated switches with low on-resistance ensure high efficiency at heavy loads while minimizing critical inductances. The MAX15112's simple layout and footprint assure first-pass success in new designs. Other features of the MAX15112 include a capacitor-programmable soft-start to reduce inrush current, safe startup into a prebiased output, an enable input, and a power-good output for power sequencing. The regulator is available in a 24-bump (4 x 6), 2.1mm x 3.05mm WLP package, and is fully specified over the -40°C to +85°C extended temperature range.

II. Manufacturing Information

A. Description/Function: High-Efficiency, 12A, Current-Mode Synchronous Step-Down Regulator with Integrated Switches

B. Process: S18

C. Number of Device Transistors: 14377

D. Fabrication Location: USA

E. Assembly Location: Japan

F. Date of Initial Production: June 24, 2011

III. Packaging Information

A. Package Type: 24-bump WLP 4x6 array

B. Lead Frame: N/A

C. Lead Finish: N/A

D. Die Attach: None

E. Bondwire: N/A (N/A mil dia.)

F. Mold Material: None

G. Assembly Diagram: #05-9000-4214

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C: Level 1

J. Single Layer Theta Ja: °C/W

K. Single Layer Theta Jc: °C/W

L. Multi Layer Theta Ja: 45°C/W

M. Multi Layer Theta Jc: °C/W

IV. Die Information

A. Dimensions: 120.08 X 82.68 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Al/0.5%Cu with Ti/TiN Barrier

D. Backside Metallization: None

E. Minimum Metal Width: 0.23 microns (as drawn)

F. Minimum Metal Spacing: 0.23 microns (as drawn)

G. Bondpad Dimensions:

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

    A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
                                                    Don Lipps (Manager, Reliability Engineering)
                                                    Bryan Preeshl (Vice President of QA)

    B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
                                                        0.1% For all Visual Defects.

    C. Observed Outgoing Defect Rate: < 50 ppm

    D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

    A. Accelerated Life Test

        The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad \text{(Chi square value for MTTF upper limit)}$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

        The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25C and 0.93 @ 55C (0.8 eV, 60% UCL)

    B. E.S.D. and Latch-Up Testing (lot SO7ZEQ002C, D/C 1135)

        The NQ63 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX15112EWG+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	SO7ZEQ002C, D/C 1135

Note 1: Life Test Data may represent plastic DIP qualification lots.