RELIABILITY REPORT

FOR

MAX15108EWP+T

WAFER LEVEL PRODUCTS

January 17, 2012

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX15108EWP+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX15108 high-efficiency, current-mode, synchronous step-down switching regulator with integrated power switches delivers up to 8A of output current. The regulator operates from 2.7V to 5.5V and provides an output voltage from 0.6V up to 95% of the input voltage, making the device ideal for distributed power systems, portable devices, and preregulation applications. The IC utilizes a current-mode control architecture with a high gain transconductance error amplifier. The current-mode control architecture facilitates easy compensation design and ensures cycle-by-cycle current limit with fast response to line and load transients. The regulator offers a selectable skip-mode functionality to reduce current consumption and achieve a higher efficiency at light output load. The low RDS(ON) integrated switches ensure high efficiency at heavy loads while minimizing critical inductance, making the layout design a much simpler task with respect to discrete solutions. The IC's simple layout and footprint assures first-pass success in new designs. The regulator features a 1MHz, factory-trimmed fixed-frequency PWM mode operation. The high switching frequency, along with the PWM current-mode architecture allows for a compact, all ceramic capacitor design. The IC features a capacitor-programmable soft-start to reduce input inrush current. Internal control circuitry ensures safe-startup into a prebiased output. Power sequencing is controlled with the enable input and power-good output. The IC is available in a 20-bump (4 x 5 array), 2.5mm x 2mm, WLP package and is fully specified over the -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	High-Efficiency, 8A, Current-Mode Synchronous Step-Down Switching Regulator
B. Process:	S18
C. Number of Device Transistors:	13122
D. Fabrication Location:	USA
E. Assembly Location:	Japan
F. Date of Initial Production:	June 16, 2011

III. Packaging Information

A. Package Type:	20-bump WLP 4x5 array
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	N/A
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	None
G. Assembly Diagram:	#05-9000-4230
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	°C/W
K. Single Layer Theta Jc:	°C/W
L. Multi Layer Theta Ja:	47°C/W
M. Multi Layer Theta Jc:	°C/W

IV. Die Information

A. Dimensions:	100.00 X 82.68 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.23 / Metal2-3 = 0.28 / Metal 4 = 2.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.23 / Metal2-3 = 0.28 / Metal 4 = 3.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.06 @ 25C and 1.04 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The NQ60-2 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2500V per JEDEC JESD22-A114 (lot SQ7XAQ002A, D/C 1126)
ESD-CDM:	+/- 750V per JEDEC JESD22-C101 (lot SQ7XAQ002B, D/C 1114)

Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78 (lot SQ7XAQ002A, D/C 1126).

Table 1
Reliability Evaluation Test Results

MAX15108EWP+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	SQ7XAQ002A, D/C 1126

Note 1: Life Test Data may represent plastic DIP qualification lots.