

RELIABILITY REPORT
FOR
MAX15024A/B+

PLASTIC ENCAPSULATED DEVICES

August 4, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR. SUNNYVALE, CA 94086

Approved by	
Ken Wendel	
Quality Assurance	
Director, Reliability Engineering	



Conclusion

The MAX15024AATB+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

Table of Contents

IDevice Description	VQuality Assurance Information		
IIManufacturing Information	VIReliability Evaluation		
IIIPackaging Information	IVDie Information		
Attachments			

I. Device Description

A. General

The MAX15024/MAX15025 single/dual, high-speed MOSFET gate drivers are capable of operating at frequencies up to 1MHz with large capacitive loads. The MAX15024 includes internal source-and-sink output transistors with independent outputs allowing for control of the external MOSFET's rise and fall time. The MAX15024 is a single gate driver capable of sinking an 8A peak current and sourcing a 4A peak current. The MAX15025 is a dual gate driver capable of sinking a 4A peak current and sourcing a 2A peak current. An integrated adjustable LDO voltage regulator provides gate-drive amplitude control and optimization. The MAX15024A/C and MAX15025A/C/E/G accept transistor-to-transistor (TTL) input logic levels while the MAX15024B/D and MAX15025B/D/F/H accept CMOS-input logic levels. High sourcing/sinking peak currents, a low propagation delay, and thermally enhanced packages make the MAX15024/MAX15025 ideal for high-frequency and high-power circuits. The MAX15024/MAX15025 operate from a 4.5V to 28V supply. A separate output driver supply input enhances flexibility and permits a soft-start of the power MOSFETs used in synchronous rectifiers. The MAX15024/MAX15025 are available in 10-pin TDFN packages and are specified over the -40°C to +125°C automotive temperature range.



II. Manufacturing Information

A. Description/Function: Single/Dual, 16ns, High Sink/Source Current Gate Drivers

B. Process: S45C. Number of Device Transistors: 1036

D. Fabrication Location: California, Texas or Japan

E. Assembly Location: Philippines, China, Thailand, Malaysia

F. Date of Initial Production: October 27, 2007

III. Packaging Information

A. Package Type: 10-pin TDFN 3x3

B. Lead Frame: Copper

C. Lead Finish: 100% matte Tin
D. Die Attach: Conductive
E. Bondwire: Au (1 mil dia.)
F. Mold Material: Epoxy with silica filler
G. Assembly Diagram: #05-9000-2966

I. Classification of Moisture Sensitivity per Level 1

JEDEC standard J-STD-020-C

H. Flammability Rating:

J. Single Layer Theta Ja: 54°C/W
K. Single Layer Theta Jc: 8.5°C/W
L. Multi Layer Theta Ja: 41°C/W
M. Multi Layer Theta Jc: 8.5°C/W

IV. Die Information

A. Dimensions: 57 X 89 mils

 $\label{eq:si3N4/SiO2} \text{Si}_3\text{N4/SiO}_2 \ \ \text{(Silicon nitride/ Silicon dioxide)}$

C. Interconnect: Al with Ti/TiN Barrier

D. Backside Metallization: None

E. Minimum Metal Width: Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
 F. Minimum Metal Spacing: Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)

Class UL94-V0

G. Bondpad Dimensions: 5 mil. Sq.
H. Isolation Dielectric: SiO₂
I. Die Separation Method: Wafer Saw



V. Quality Assurance Information

A. Quality Assurance Contacts: Ken Wendel (Director, Reliability Engineering)

Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppmD. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = 1$$
 = 1.83 (Chi square value for MTTF upper limit)
 $192 \times 4340 \times 48 \times 2$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$x = 22.4 \times 10^{-9}$$

3 = 22.4 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maximic.com/. Current monitor data for the S45 Process results in a FIT Rate of 2.33 @ 25C and 28.16 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The NQ07 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000 V per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of +/-250 mA.



Table 1

Reliability Evaluation Test Results

MAX15024AATB+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	
Static Life Test ((Note 1)				
	Ta = 135°C	DC Parameters	48	0	
	Biased	& functionality			
	Time = 192 hrs.				
Moisture Testing	(Note 2)				
85/85	Ta = 85°C	DC Parameters	77	0	
	RH = 85%	& functionality			
	Biased	·			
	Time = 1000hrs.				
Mechanical Stres	ss (Note 2)				
Temperature	-65°C/150°C	DC Parameters	77	0	
Cycle	1000 Cycles	& functionality			
	Method 1010				

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data