RELIABILITY REPORT

FOR

MAX1489ExxD

PLASTIC ENCAPSULATED DEVICES

December 29, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX1489E successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description

II.Manufacturing Information

III.Packaging Information

IV.Die Information

V.Quality Assurance Information

VI.Reliability Evaluation

VI.Reliability Evaluation

VI.Attachments

I. Device Description

A. General

The MAX1489E quad, low-power line receiver is designed for EIA/TIA-232, EIA/TIA-562, and CCITT V.28 communications in harsh environments. Each receiver input is protected against $\pm 15 \text{kV}$ electrostatic discharge (ESD) shocks. These inputs have a $\pm 25 \text{V}$ range and feature hysteresis and time-domain filtering. The outputs are TTL and CMOS compatible. The MAX1489E has a 120kbps guaranteed data rate. Supply current is typically $350 \mu A$.

The MAX1489E is pin compatible with the MC1489, MC14C89, SN75189, SN75C189, DS1489, and DS14C89.

B. Absolute Maximum Ratings

<u>ltem</u>	Rating
Supply Voltage (V_{CC}) Input Voltage (V_{IN}) Output Short-Circuit Current (Shorted to GND or V_{CC}) (Note 1) Storage Temp.	+7V ±30V Self Limiting -65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation ($TA = +70^{\circ}C$)	
14-Pin PDIP	800mW
14-Pin NSO	695mW
Derates above +70°C	
14-Pin PDIP	10.0W/°C
14-Pin NSO	8.7W/°C

Note 1: Only one output may be shorted at a time.

II. Manufacturing Information

A. Description/Function: ±15kV ESD-Protected, Quad, Low-Power RS-232 Line Receiver

B. Process: M5 ((SMG) - 5 micron metal gate CMOS)

C. Number of Device Transistors: 144

D. Fabrication Location: Oregon, USA

E. Assembly Location: Philippines, Malaysia, or Thailand

F. Date of Initial Production: November, 1995

III. Packaging Information

A. Package Type: 14-Lead SO 14-Lead PDIP

B. Lead Frame: Copper Copper

C. Lead Finish: Solder Plate Solder Plate

D. Die Attach: Silver-filled Epoxy Silver-filled Epoxy

E. Bondwire: Gold (1.3 mil dia.) Gold (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler Epoxy with silica filler

G. Assembly Diagram: # 05-1901-0119 # 05-1901-0118

H. Flammability Rating: Class UL94-V0 Class UL94-V0

I. Classification of Moisture Sensitivity

per JEDEC standard JESD22-A112: Level 1 Level 1

IV. Die Information

A. Dimensions: 71 x 96 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 5 microns (as drawn)

F. Minimum Metal Spacing: 5 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO₂

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA)

Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 160 \times 2}$$
 (Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

 $\lambda = 6.79 \times 10^{-9}$ $\lambda = 6.79 \text{ F.I.T.}$ (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. # 06-5143) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR-1M).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The RS32 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Additionally, the MAX1489E's I/O pins are ESD-protected to ±15kV using the IEC 1000-4-2, Air-Gap Discharge Method, ±15kV using the Human Body Model, and ±8kV using the IEC 1000-4-2, Contact Discharge Method.

Latch-Up testing has shown that this device withstands a current of ±100mA.

Table 1 Reliability Evaluation Test Results

MAX1489ExxD

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	t (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		160	0
Moisture Testi	ng (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	DIP SO	77 77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Str	ress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots. Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/2/

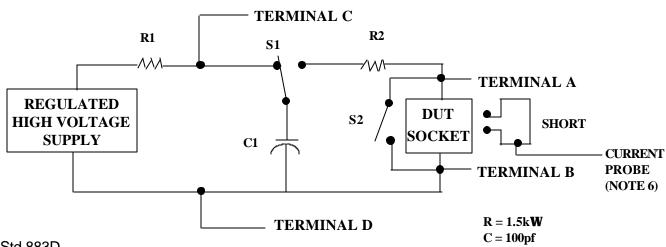
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)			
1.	All pins except V _{PS1} 3/	All V _{PS1} pins			
2.	All input and output pins	All other input-output pins			

- 1/ Table II is restated in narrative form in 3.4 below.
- 2/ No connects are not to be tested.
- 3/ Repeat pin combination I for each named Power supply and for ground

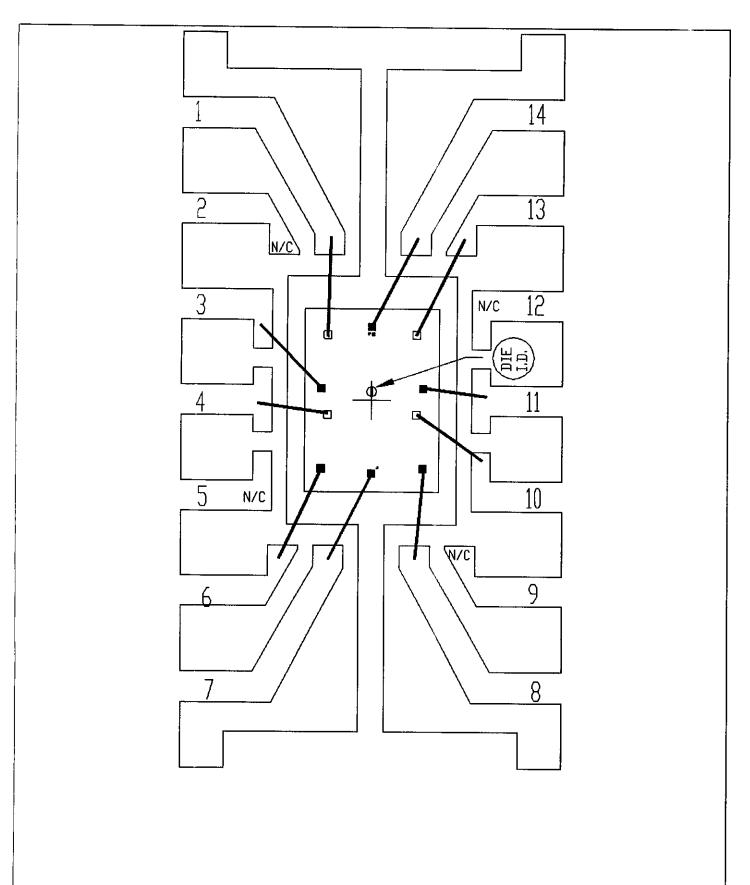
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_{S}$, $-V_{S}$, V_{REF} , etc).

3.4 Pin combinations to be tested.

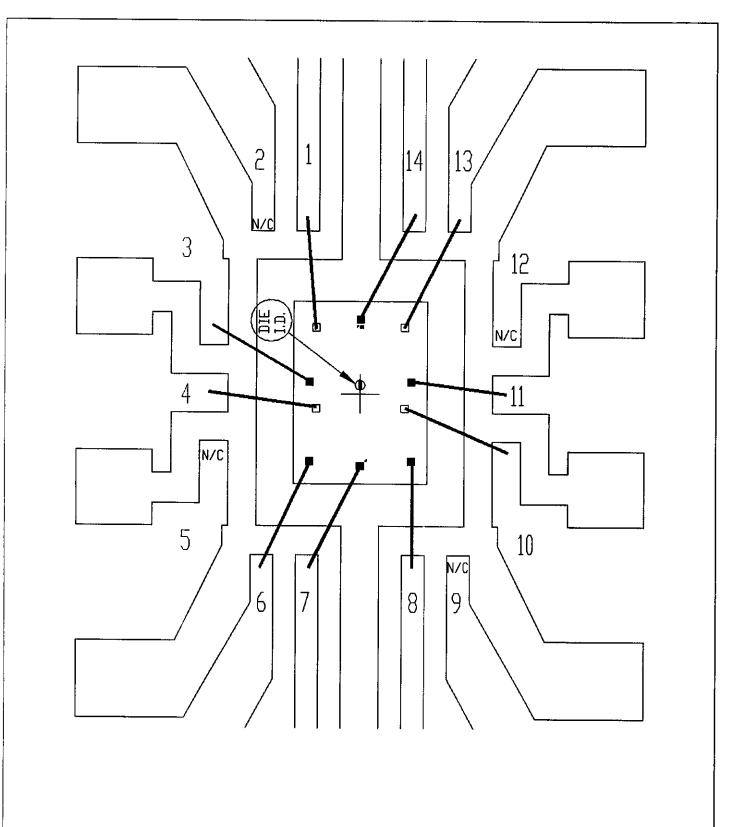
- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{S1}, or V_{S2} or V_{S3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D Method 3015.7 Notice 8



PKG,CODE: \$14-2		APPROVALS	DATE	MAXI	/VI
CAV./PAD SIZE: 90 X 130	PKG. DESIGN			BUILDSHEET NUMBER: 05-1901-0119	REV.i



PKG.CODE:	P14-3				
CAV./PAD	SIZE	v	140	PKG.	Ī
	110	X	140	DESIGN	

APPROVALS

DATE

BUILDSHEET NUMBER: REV.:

А

05-1901-0118

