RELIABILITY REPORT

FOR

MAX14850ASE+

PLASTIC ENCAPSULATED DEVICES

August 14, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
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Conclusion

The MAX14850ASE+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14850 is a six-channel digital isolator utilizing Maxim's proprietary process technology, whose monolithic design provides a compact and low-cost transfer of digital signals between circuits with different power domains. The technology enables low power consumption and stable high-temperature performance. The four unidirectional channels are each capable of DC to 50Mbps, with two of the four channels passing data across the isolation barrier in each direction. The two bidirectional channels are open drain and each is capable of data rates from DC to 2Mbps. Independent 3.0V to 5.5V supplies on each side of the isolator also make it suitable for use as a level translator. The MAX14850 can be used for isolating SPI busses, I²C busses with clock stretching, RS-232, RS-485/RS-422 busses, and general-purpose isolation. When used as a bus isolator, extra channels are available for power monitoring and reset signals. The MAX14850 is available in a narrow body, 16-pin SO (10mm x 4mm) package. The SO package is specified over the -40°C to +125°C automotive temperature range.

II. Manufacturing Information

A. Description/Function:	Six-Channel Digital Isolator
B. Process:	DM200
C. Number of Device Transistors:	8116
D. Fabrication Location:	Oregon
E. Assembly Location:	Malaysia, Philippines, or Thailand
F. Date of Initial Production:	March 26, 2012

III. Packaging Information

A. Package Type:	16-pin SOIC (N)
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4525
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	115°C/W
K. Single Layer Theta Jc:	32°C/W
L. Multi Layer Theta Ja:	75°C/W
M. Multi Layer Theta Jc:	24°C/W

IV. Die Information

A. Dimensions:	69.685X83.4645 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.8 microns
F. Minimum Metal Spacing:	Metal1 = 2.0 microns
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the DM200 Process results in a FIT Rate of 0.92 @ 25C and 1 5 .8 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot JAAI0Q002D, D/C 1147)

The RU57 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX14850ASE+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	JAAI0Q002E, D/C 1147

Note 1: Life Test Data may represent plastic DIP qualification lots.