

RELIABILITY REPORT
FOR
MAX14842ATE+
PLASTIC ENCAPSULATED DEVICES

September 29, 2014

MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

| |
|----------------------|
| Approved by |
| Sokhom Chum |
| Quality Assurance |
| Reliability Engineer |

Conclusion

The MAX14842ATE+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

| | |
|--|---|
| I.Device Description | IV.Die Information |
| II.Manufacturing Information | V.Quality Assurance Information |
| III.Packaging Information | VI.Reliability Evaluation |
|Attachments | |

I. Device Description

A. General

The MAX14842 translates digital signals between two domains that have different ground references of up to 72V. The device features six communication channels, two bidirectional and four unidirectional. Two of the four unidirectional channels go in each direction. The device is powered by two supply voltages that independently define the logic levels of each ground domain. The MAX14842 supports guaranteed data rates up to 30Mbps on the four unidirectional channels and up to 2Mbps on the two bidirectional channels. The bidirectional channels have open-drain outputs, making them suitable for I²C signals. I²C clock stretching and hot swapping is supported on the bidirectional channels. Undervoltage lockout ensures that the output pins have a defined behavior during power-up, power-down, and during supply transients. For proper operation, ensure that 0V GNDB - VGND(A) ≤ 72V. Note that GNDB must be greater than or equal to GNDA. The MAX14842 is available in a 16-pin TQFN package and is specified over the -40°C to +125°C automotive temperature range.

II. Manufacturing Information

| | |
|----------------------------------|--|
| A. Description/Function: | 6-Channel, Digital Ground-Level Translator |
| B. Process: | S45 |
| C. Number of Device Transistors: | 656 |
| D. Fabrication Location: | California, Texas or Japan |
| E. Assembly Location: | Taiwan, China, Thailand |
| F. Date of Initial Production: | March 28, 2012 |

III. Packaging Information

| | |
|--|--------------------------|
| A. Package Type: | 16-pin TQFN 4x4 |
| B. Lead Frame: | Copper |
| C. Lead Finish: | 100% matte Tin |
| D. Die Attach: | Conductive |
| E. Bondwire: | Au (0.8 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | #05-9000-4245 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1 |
| J. Single Layer Theta Ja: | 59.3°C/W |
| K. Single Layer Theta Jc: | 5.7°C/W |
| L. Multi Layer Theta Ja: | 40°C/W |
| M. Multi Layer Theta Jc: | 5.7°C/W |

IV. Die Information

| | |
|----------------------------|---|
| A. Dimensions: | 52X57 mils |
| B. Passivation: | Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Al/0.5%Cu with Ti/TiN Barrier |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | Metal1 = 0.5 microns (as drawn) |
| F. Minimum Metal Spacing: | Metal1 = 0.45 microns (as drawn) |
| G. Bondpad Dimensions: | |
| H. Isolation Dielectric: | SiO ₂ |
| I. Die Separation Method: | Wafer Saw |

V. Quality Assurance Information

- A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{1000 \times 4340 \times 46 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 8.12 \times 10^{-9}$$

$\lambda = 8.12$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.04 @ 25C and 0.69 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (ESD lot TQ0ZCQ002A D/C 1117, Latch-Up lot TQ0ZBQ001D D/C 1104)

The RU50 die type has been found to have all pins able to withstand a transient pulse of:

| | |
|----------|---------------------------------|
| ESD-HBM: | +/- 1500V per JEDEC JESD22-A114 |
| ESD-CDM: | +/- 750V per JEDEC JESD22-C101 |

Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX14842ATE+

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES | COMMENTS |
|----------------------------------|--|----------------------------------|-------------|--------------------|----------------------|
| Static Life Test (Note 1) | Ta = 135°C Biased Time = 1000 hrs. | DC Parameters & functionality | 46 | 0 | TQ0ZCQ002F, D/C 1241 |

Note 1: Life Test Data may represent plastic DIP qualification lots