



RELIABILITY REPORT  
FOR  
MAX14824ETG+T  
PLASTIC ENCAPSULATED DEVICES

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**MAXIM INTEGRATED PRODUCTS**

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## Conclusion

The MAX14824ETG+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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## I. Device Description

### A. General

The MAX14824 is an IO-Link® master interface that integrates an IO-Link physical layer transceiver with an auxiliary digital input and two linear regulators. High port count IO-Link master applications are supported through in-band SPI addressing, and the 12MHz SPI interface minimizes host controller access times. In-band addressing and selectable SPI addresses enable cascading up to 16 devices. The device supports all the IO-Link data rates and features slew-rate-controlled drivers to reduce EMI. The driver is guaranteed to drive up to 300mA (min) load currents. Internal wake-up circuitry automatically determines the correct wake-up polarity, allowing for the use of simple UARTs for wake-up pulse generation. The MAX14824 is available in a 4mm x 4mm, 24-pin TQFN package with exposed pad, and operates over the extended -40°C to +105°C temperature range.

**II. Manufacturing Information**

A. Description/Function:	IO-Link Master Transceiver
B. Process:	S4
C. Number of Device Transistors:	15024
D. Fabrication Location:	Texas
E. Assembly Location:	Taiwan, China, Thailand, Malaysia
F. Date of Initial Production:	September 8, 2011

**III. Packaging Information**

A. Package Type:	24L TQFN
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3925 / A
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	48°C/W
K. Single Layer Theta Jc:	3°C/W
L. Multi Layer Theta Ja:	36°C/W
M. Multi Layer Theta Jc:	3°C/W

**IV. Die Information**

A. Dimensions:	100X100 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)  
Don Lipps (Manager, Reliability Engineering)  
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 96 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 11.4 \times 10^{-9}$$

$$\lambda = 11.4 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the S4 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

### B. E.S.D. and Latch-Up Testing (lot SC6YEQ003B D/C 1118)

The RU45-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

**Table 1**  
Reliability Evaluation Test Results

**MAX14824ETG+T**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
<b>Static Life Test</b> (Note 1)	Ta = 135°C	DC Parameters	48	0	SC6YDA004A, D/C 1048
	Biased	& functionality	48	0	SC6ZDA004A, D/C 1048
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.