RELIABILITY REPORT

FOR

MAX14802CCM+ / MAX14802ECM+

PLASTIC ENCAPSULATED DEVICES

April 27, 2017

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX14802CCM+ / MAX14802ECM+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX14802/MAX14803/MAX14803A provide high-voltage switching on 16 channels for ultrasonic imaging and printer applications. The devices utilize HVCMOS process technology to provide 16 high-voltage low-charge-injection SPST switches, controlled by a digital interface. Data is clocked into an internal 16-bit shift register and retained by a programmable latch with enable and clear inputs. A power-on reset function ensures that all switches are open on power-up. The MAX14802/MAX14803/MAX14803A operate with a wide range of high-voltage supplies including VPP/VNN = +100V/-100V, +200V/0V, or +40V/-160V. The digital interface operates from a separate +2.7V to +5.5V VDD supply. Digital inputs DIN, CLK, active-low LE, and CLR operate on the VDD supply voltage. The MAX14803/MAX14803A provide integrated 35k bleed resistors on each switch terminal to discharge capacitive loads. The MAX14802/MAX14803/MAX14803A provide integrated clamping diodes for overvoltage protection against positive overshoot. The MAX14802/MAX14803 are available in the 48-pin TQFP package and are specified for the commercial 0°C to +70°C temperature range. The MAX14803A is available in the 110-bump wafer level package (WLP) and is specified at the -40°C to +85°C temperature range.

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II. Manufacturing Information

A. Description/Function:	Low-Charge-Injection, 16-Channel, High-Voltage Analog Switches
B. Process:	BCD250
C. Number of Device Transistors:	1417
D. Fabrication Location:	USA
E. Assembly Location:	Malaysia
F. Date of Initial Production:	April 25, 2009

III. Packaging Information

A. Package Type:	48-pin LQFP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3436
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	°C/W
K. Single Layer Theta Jc:	°C/W
L. Multi Layer Theta Ja:	44°C/W
M. Multi Layer Theta Jc:	10°C/W

IV. Die Information

A. Dimensions:	214 X 214 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 1.5µm / Metal2 = 3.0µm
F. Minimum Metal Spacing:	Metal1 = 1.5µm / Metal2 = 3.0µm
G. Isolation Dielectric:	SiO_2
H. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Eric Wright (Reliability Engineering)
Brian Standley (Manager, Reliability)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

λ = 22.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the BCD250 Process results in a FIT Rate of 0.43 @ 25C and 7.42 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The AJ47-2 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 600V per JEDEC JESD22-A114 (lot NRSXDQ003A, D/C 0929). Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78 (lot NRSXC3001A, D/C 0913).

Table 1
Reliability Evaluation Test Results

MAX14802CCM+ / MAX14802ECM+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	NRSXDQ003C, D/C 0929

Note 1: Life Test Data may represent plastic DIP qualification lots.

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