RELIABILITY REPORT

FOR

MAX14689ETP+T / MAX14689EWL+T

PLASTIC ENCAPSULATED DEVICES

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MAXIM INTEGRATED

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Conclusion

The MAX14689ETP+T / MAX14689EWL+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14689 ultra-small, low-on-resistance (RON) double-pole/double-throw (DPDT) analog switches feature Beyond-the-Rails™ capability that allows signals from -5.5V to +5.5V to pass without distortion, even when the power supply is below the signal range. The low on-resistance (0.25Ω) also makes the device ideal for low-distortion switching applications, such as audio or video. The MAX14689 is fully specified to operate from a single +1.6V to +5.5V power supply. Because of the low supply current requirement, VCC can be provided by a GPIO. When power is not applied, the switches go to a high-impedance mode and all analog signal ports can withstand signals from -5.5V to +5.5V. The switch is controlled with a single control bit, CB. The MAX14689 is available in a 1.2mm x 1.2mm, 0.4mm pitch, 9-bump wafer-level package (WLP), and operate over the -40°C to +85°C extended temperature range.

II. Manufacturing Information

A. Description/Function:	Ultra-Small, Low-RON, Beyond-the-Rails DPDT Analog Switches
B. Process:	S18
C. Number of Device Transistors:	3077
D. Fabrication Location:	USA
E. Assembly Location:	Taiwan, China, Thailand
F. Date of Initial Production:	September 26, 2013

III. Packaging Information

A. Package Type:	20-pin TQFN 4x4	9-bmp WLP 3x3
B. Lead Frame:	Copper	N/A
C. Lead Finish:	100% matte Tin	N/A
D. Die Attach:	Conductive	None
E. Bondwire:	Au (0.8 mil dia.)	N/A
F. Mold Material:	Epoxy with silica filler	None
G. Assembly Diagram:	#05-9000-5387	#05-9000-5386
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	59°C/W	N/A°C/W
K. Single Layer Theta Jc:	6°C/W	N/A°C/W
L. Multi Layer Theta Ja:	39°C/W	83°C/W
M. Multi Layer Theta Jc:	6°C/W	N/A°C/W

IV. Die Information

A. Dimensions:	50 X 50 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25°C and 0.93 @ 55°C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot EANA9Q002A, D/C1322)

The AL68-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX14689ETP+T / MAX14689EWL+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	EANA9Q002A, D/C1322

Note 1: Life Test Data may represent plastic DIP qualification lots.