RELIABILITY REPORT

FOR

MAX14640ETA+T

PLASTIC ENCAPSULATED DEVICES

March 19, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Richard Aburano
Quality Assurance
Manager, Reliability Engineering

Conclusion

The MAX14640ETA+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14640-MAX14644/MAX14651 are next-generation USB 2.0 host charger adapter emulators that combine USB Hi-Speed analog switches with a USB adapter emulator circuit. The MAX14640/MAX14651 feature an I²C interface to fully configure the charging behavior with different address options. The MAX14641-MAX14644 are controlled by two GPIO inputs (CB1/CB0) and support USB data and automatic charger mode. In charging downstream port (CDP) pass-through mode, the devices emulate the CDP function while supporting normal USB traffic. The MAX14641/MAX14642/MAX14643 have a CEN output for an active-high CLS enable input, and the MAX14644 has an active-low CEN output for an active-low CLS enable input to restart the peripheral connected to the USB host. The MAX14640-MAX14644/MAX14651 feature 2A high-current autodetect mode. The MAX14641 features 1A high-current forced mode instead of regular DCP mode. The MAX14640/MAX14651 can be configured through I²C to support various dedicated charger modes such as DCP, Apple® 1A/2A forced, or Apple 1A/2A automatic mode. All the devices support CDP and standard downstream port (SDP) charging while in the active state (S0) and support the dedicated charging port (DCP) charging while in the standby state (S3/S4/S5). All devices support low-speed remote wake-up by monitoring DM, and the MAX14642 also supports remote wake-up in sleep mode (S3). The MAX14640-MAX14644/MAX14651 are available in an 8-pin (2mm x 2mm) TDFN-EP package and are specified over the -40°C to +85°C extended temperature range.

II. Manufacturing Information

A. Description/Function:	USB Host Adapter Emulators
B. Process:	S18
C. Number of Device Transistors:	29841
D. Fabrication Location:	USA
E. Assembly Location:	China, Taiwan and Thailand
F. Date of Initial Production:	September 27, 2012

III. Packaging Information

A. Package Type:	8-pin TDFN 2x2
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4982
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	110°C/W
K. Single Layer Theta Jc:	8°C/W
L. Multi Layer Theta Ja:	83.9°C/W
M. Multi Layer Theta Jc:	8°C/W

IV. Die Information

A. Dimensions:	34.6457X46.063 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 79 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.9 \times 10^{-9}$

$\lambda = 13.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25C and 0.93 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SAFZ4Q001D, D/C 1220)

The AL50-0 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX14640ETA+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	79	0	SAFZ4Q001D, D/C 1220

Note 1: Life Test Data may represent plastic DIP qualification lots.