RELIABILITY REPORT

FOR

MAX14604ETA+T

PLASTIC ENCAPSULATED DEVICES

September 29, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX14604ETA+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX14600-MAX14605 are third-generation USB 2.0 host charger identification devices that combine USB Hi-Speed analog switches with a USB adapter emulator circuit. The devices support pass-through mode and auto mode. In charging downstream port (CDP) pass-through mode, the devices emulate the CDP function while supporting normal USB traffic. The MAX14600/MAX14603/MAX14605 have a pFET open-drain output (active-low CEN), and the MAX14601/MAX14604 have an nFET open-drain output (CEN) to restart the peripheral connected to the USB host. All the devices support the CDP and standard downstream port (SDP) charging during the active state (S0) and support the dedicated charging port (DCP) charging during the standby state (S3/S4/S5). The MAX14603/MAX14604/MAX14605 support remote wake-up in standby mode. The MAX14602/MAX14605 offer backward-compatible CDP emulation upgrade to the MAX14566E. The MAX14600-MAX14605 are available in an 8-pin (2mm x 2mm) TDFN package, and are specified over the -40°C to +85°C extended temperature range.

II. Manufacturing Information

A. Description/Function:	USB Host Charger Identification/Adapter Emulators
B. Process:	S18
C. Number of Device Transistors:	21666
D. Fabrication Location:	California
E. Assembly Location:	Taiwan
F. Date of Initial Production:	July 5, 2011

III. Packaging Information

A. Package Type:	TDFN 2x2 8L
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4574 / A
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	110°C/W
K. Single Layer Theta Jc:	37°C/W
L. Multi Layer Theta Ja:	83.9°C/W
M. Multi Layer Theta Jc:	37°C/W

IV. Die Information

A. Dimensions:	33.07X44.49 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18µm
F. Minimum Metal Spacing:	0.18µm
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{240 \times 4340 \times 80 \times 2} \quad \text{(Chi square value for MTTF upper limit)}$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 11.0 \times 10^{-9}$

λ = 11.0 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot S2GVAQ001B D/C 1118)

The AL24-4 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX14604ETA+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 240 hrs.	DC Parameters & functionality	80	0	S2GXAQ001B, D/C 1118

Note 1: Life Test Data may represent plastic DIP qualification lots.