RELIABILITY REPORT

FOR

MAX14550EETB+

PLASTIC ENCAPSULATED DEVICES

July 28, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Conclusion

The MAX14550EETB+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX14550E is a USB Hi-Speed analog switch with a USB host charger (dedicated charger) identification circuit. The MAX14550E supports both the USB Battery Charging Specification Revision 1.0 and a set resistor bias for AppleM-compliant devices.

The MAX14550E features a high-performance Hi-Speed USB switch with low 4pF (typ) on-capacitance and low 4I (typ) on-resistance. In addition, the MAX14550E features two digital inputs (CB0 and CB1) to switch between pass-through and charger modes. The USB host charger identification circuit allows a host USB port to support USB chargers with shorted D+/D- detection and to provide support for Apple-compliant devices using a resistor bias. When an Apple device is attached to the port, the MAX14550E provides the voltage from the external divider. If a USB Revision 1.0-compliant device is attached, the MAX14550E connects a short across DP and DM to allow correct charger detection. The MAX14550E auto-detection circuit can be disabled and either a DP/DM short or resistor network chosen as the default.

The MAX14550E has enhanced high electrostatic discharge (ESD) protection on the DP and DM inputs up to Q15kV Human Body Model (HBM). The MAX14550E is available in a 10-pin (3mm x 3mm) TDFN package and is specified over the -40NC to +85NC extended temperature range.

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II. Manufacturing Information

A. Description/Function:	USB Host Charger Identification Analog Switch
B. Process:	S4
C. Number of Device Transistors:	1683
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	Thailand
F. Date of Initial Production:	

III. Packaging Information

A. Package Type:	10-pin TDFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Au (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	54°C/W
K. Single Layer Theta Jc:	8.5°C/W
L. Multi Layer Theta Ja:	41°C/W
M. Multi Layer Theta Jc:	8.5°C/W

IV. Die Information

A. Dimensions:	31 X 47 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the S4 Process results in a FIT Rate of 4.6 @ 25C and 79.2 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The AJ99 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500 V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250 mA, 1.5x VCCMax Overvoltage per JESD78.

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Table 1
Reliability Evaluation Test Results

MAX14550EETB+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

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