RELIABILITY REPORT

FOR

MAX14531EEWC+

WAFER LEVEL PRODUCTS

June 8, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

Conclusion

The MAX14531EEWC+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14531E-MAX14534E high ESD-protected DP3T switches multiplex Hi-Speed (480Mbps) USB signals, low/full-speed USB signals, and analog signals such as AC-coupled audio or video through any of three channels. These devices combine the low on-capacitance (CON) and low on-resistance (RON) necessary for high-performance switching applications in portable electronics, and include an internal negative supply to pass AC-coupled audio signals that swing below ground (down to -2.0V). The MAX14531E-MAX14534E operate from a +2.7V to +5.5V supply. The MAX14531E-MAX14534E have a shutdown function to reduce supply current and set all channels to high impedance. The MAX14531E-MAX14534E feature a VBUS detection function through the CB0 input to automatically switch to the default USB signal path upon detection of a valid VBUS signal. The MAX14532E/MAX14534E feature internal shunt resistors on audio channels to reduce clicks and pops heard at the output. The MAX14531E-MAX14534E are available in a space-saving, 12-bump, 1.5mm x 2.0mm WLP package and operate over the -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	USB 2.0 Hi-Speed and Audio Switches with Negative Signal Capability and ±15kV ESD
B. Process:	S45
C. Number of Device Transistors:	1790
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	Japan
F. Date of Initial Production:	April 24, 2009

III. Packaging Information

A. Package Type:	12 bmp WLP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3573
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	62°C/W
M. Multi Layer Theta Jc:	N/A

IV. Die Information

A. Dimensions:	84X61 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.13 @ 25C and 2.31 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot TTQZBQ002A, D/C 1026)

The AJ83 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX14531EEWC+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	TTQZBQ002D, D/C 1026

Note 1: Life Test Data may represent plastic DIP qualification lots.