RELIABILITY REPORT

FOR

MAX1449EHJ+

PLASTIC ENCAPSULATED DEVICES

January 13, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX1449EHJ+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1449 3.3V, 10-bit analog-to-digital converter (ADC) features a fully differential input, a pipelined 10-stage ADC architecture with wideband track-and-hold (T/H), and digital error correction incorporating a fully differential signal path. The ADC is optimized for lowpower, high-dynamic performance in imaging and digital communications applications. The converter operates from a single 2.7V to 3.6V supply, consuming only 186mW while delivering a 58.5dB (typ) signal-to-noise ratio (SNR) at a 20MHz input frequency. The fully differential input stage has a -3dB 400MHz bandwidth and may be operated with single-ended inputs. In addition to low operating power, the MAX1449 features a 5µA power-down mode for idle periods. An internal 2.048V precision bandgap reference is used to set the ADC's full-scale range. A flexible reference structure allows the user to supply a buffered, direct, or externally derived reference for applications requiring increased accuracy or a different input voltage range. See a parametric table of the complete family of pin-compatible, 10-bit high-speed ADCs in the datasheet. The MAX1449 has parallel, offset binary, CMOS-compatible, three-state outputs that can be operated from 1.7V to 3.6V to allow flexible interfacing. The device is available in a 5mm x 5mm 32-pin TQFP package and is specified over the extended industrial (-40°C to +85°C) temperature range.

II. Manufacturing Information

A. Description/Function:	10-Bit, 105Msps, Single +3.3V, Low-Power ADC with Internal Reference
B. Process:	0.35UM 2 Poly 3 Metal CMOS (TS352P3M)
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	ATP Philippines, Carsem Malaysia
F. Date of Initial Production:	October 21, 2000

III. Packaging Information

A. Package Type:	32-pin TQFP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-2101-0024
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Multi Layer Theta Ja:	53.5°C/W

IV. Die Information

A. Dimensions:	85 X 87 mils
B. Passivation:	Silicon Dioxide/Silicon Nitride
C. Interconnect:	Al/Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35 um
F. Minimum Metal Spacing:	0.35 um
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	Silicon Dioxide
I. Die Separation Method:	Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 289 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 3.7 \times 10^{-9}$

$\lambda = 3.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the TS352P3M Process results in a FIT Rate of 0.43 @ 25C and 7.50 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The AC12 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500 V per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX1449EHJ+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	289	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data