

RELIABILITY REPORT

FOR

MAX14483AAP+

MAX14483AAP+T

PLASTIC ENCAPSULATED DEVICE

December 10, 2018

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134



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Conclusion

The MAX14483 successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14483 is a 6-channel, 3.75kVRMS digital galvanic isolator using Maxim's proprietary process technology. The six signal channels are individually optimized for SPI applications and include very low propagation delay on the SDI, SDO, and SCLK channels. The SDO channel's tri-state control is enabled by the CS input as well as a second enable control input pin (SDOEN), allowing a single MAX14483 to isolate multiple SPI devices. To simplify system design, an open drain FAULT output can be wire ORed with error outputs from other devices. In addition, an auxiliary channel (AUX) is available for passing timing or control signals from the master side to the slave side and power monitors (SAA, SBA) are provided for both power domains to signal if the opposite side of the isolator is ready for operation. Independent 1.71V to 5.5V supplies on each side of the isolator also make the device suitable for use as a level translator.

II. Manufacturing Information

A. Description/Function:	6-Channel, Low-Power, 3.75kVRMS SPI Digital Isolator
B. Process:	S18
C. Device count:	2 x 23474 (2 RV64A die)
D. Fabrication Location:	USA
E. Assembly Location:	Thailand
F. Date of Initial Production:	February 22, 2018

III. Packaging Information

A. Package Type:	SSOP Hybrid
B. Lead Frame:	Cu194
C. Lead Finish:	Matte Tin
D. Die Attach:	AB8200T
E. Bondwire:	Au (1.00 mil dia.)
F. Mold Material:	G605L
G. Assembly Diagram:	05-100550
H. Flammability Rating:	UL-94 (V-0 Rating)
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	125 °C/W
K. Single Layer Theta Jc:	33 °C/W
L. Multi Layer Theta Ja:	83 °C/W
M. Multi Layer Theta Jc:	33 °C/W

IV. Die Information

A. Dimensions:	40.1575X105.1181 mils (RV64A die size)
B. Passivation:	Si ₃ N ₄ /SiO ₂

V. Quality Assurance Information

A. Quality Assurance Contacts:	Norbert Gerena (Engineer, Reliability) Brian Standley (Manager, Reliability) Bryan Preeshl (SVP of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 125C biased (static) life test are shown in Table 1. Using these results, the Failure Rate λ is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{1000 \times 2454 \times 237 \times 2} \text{ (Chi square value for MTTF upper limit)}$$

(where 2454 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 4.73 \times 10^{-9}$$

$$\lambda = 4.73 \text{ FITs (60\% confidence level @25°C)}$$

Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <https://www.maximintegrated.com/en/support/qa-reliability/reliability/reliability-monitor-program.html>.

MFN S18 Quarterly Process FIT from Q2FY18

$$\lambda = 0.1 \text{ FITs (60\% confidence level @25°C)}$$

B. E.S.D. and Latch-Up Testing

The MAX14483 has been found to have all pins able to withstand an HBM transient pulse of +/- 2500 V per JEDEC / ESDA JS-001. Latch-Up testing has shown that this device withstands +/- 250 mA current injection and supply overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results
MAX14483AAP+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 125C	DC Parameters & functionality	79 x 3 lots	0	
	Biased Time = 1000 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.