RELIABILITY REPORT

FOR

MAX1437BETK+

PLASTIC ENCAPSULATED DEVICES

January 9, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
Ken Wendel
Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX1437BETK+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1437B octal, 12-bit analog-to-digital converter (ADC) features fully differential inputs, a pipelined architecture, and digital error correction incorporating a fully differential signal path. This ADC is optimized for low-power and high-dynamic performance in medical imaging instrumentation and digital communications applications. The MAX1437B operates from a 1.8V single supply and consumes only 768mW (96mW per channel) while delivering a 70.2dB (typ) signal-to-noise ratio (SNR) at a 5.3MHz input frequency. In addition to low operating power, the MAX1437B features a low-power standby mode for idle periods. An internal 1.24V precision bandgap reference sets the full-scale range of the ADC. A flexible reference structure allows the use of an external reference for applications requiring increased accuracy or a different input voltage range. The reference architecture is optimized for low noise. A single-ended clock controls the data-conversion process. An internal duty-cycle equalizer compensates for wide variations in clock duty cycle. An on-chip phase-locked loop (PLL) generates the high-speed serial low-voltage differential signal (LVDS) clock. The MAX1437B has self-aligned serial LVDS outputs for data, clock, and frame-alignment signals. The output data is presented in two's complement format. The MAX1437B offers a maximum sample rate of 50Msps. This device is available in a small, 10mm x 10mm x 0.8mm, 68-pin thin QFN package with exposed pad and is specified for the extended industrial (-40°C to +85°C) temperature range.

II. Manufacturing Information

A. Description/Function:	Octal, 12-Bit, 50Msps, 1.8V ADC with Serial LVDS Outputs
B. Process:	TSMC 0.18 um, 1 Poly, 4 Metal CMOS
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	UTL Thailand
F. Date of Initial Production:	7/25/2008

III. Packaging Information

A. Package Type:	68-pin TQFN 10x10
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	34°C/W
K. Single Layer Theta Jc:	0.3°C/W
L. Multi Layer Theta Ja:	20°C/W
M. Multi Layer Theta Jc:	0.3°C/W

IV. Die Information

A. Dimensions:	276 X 254 mils
B. Passivation:	Laser/TEOS Ox - Pass/Nit -PreLP+GenLP
C. Interconnect:	Al/Cu 0.5%
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 160 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 6.7 \times 10^{-9}$

λ = 6.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the TSMC 0.18um Process results in a FIT Rate of 0.8 @ 25C and 13.1 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The CA14-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500 V per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of +/-250 mA, 1.5x VCCMax Overvoltage per JESD78.

Table 1
Reliability Evaluation Test Results

MAX1437BETK+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135 Biased Time = 192 hrs.	DC Parameters & functionality	160	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data