RELIABILITY REPORT

FOR

MAX1436BECQ+D

PLASTIC ENCAPSULATED DEVICES

December 14, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX1436BECQ+D successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1436B octal, 12-bit analog-to-digital converter (ADC) features fully differential inputs, a pipelined architecture, and digital error correction incorporating a fully differential signal path. This ADC is optimized for low-power and high-dynamic performance in medical imaging instrumentation and digital communications applications. The MAX1436B operates from a 1.8V single supply and consumes only 743mW (93mW per channel) while delivering a 69.9dB (typ) signal-to-noise ratio (SNR) at a 5.3MHz input frequency. In addition to low operating power, the MAX1436B features a low-power standby mode for idle periods. An internal 1.24V precision bandgap reference sets the full-scale range of the ADC. A flexible reference structure allows the use of an external reference for applications requiring increased accuracy or a different input voltage range. The reference architecture is optimized for low noise. A single-ended clock controls the data-conversion process. An internal duty-cycle equalizer compensates for wide variations in clock duty cycle. An on-chip PLL generates the high-speed serial low-voltage differential signal (LVDS) clock. The MAX1436B has self-aligned serial LVDS outputs for data, clock, and frame-alignment signals. The output data is presented in two's complement or binary format. The MAX1436B offers a maximum sample rate of 40Msps. See the *Pin-Compatible Versions* table in the full data sheet for higher-speed versions. This device is available in a small, 14mm x 14mm x 1mm, 100-pin TQFP package with exposed pad and is specified for the extended industrial (-40°C to +85°C) temperature range.

II. Manufacturing Information

A. Description/Function:	Octal, 12-Bit, 40Msps, 1.8V ADC with Serial LVDS Outputs
B. Process:	TS18
C. Number of Device Transistors:	190000
D. Fabrication Location:	Taiwan
E. Assembly Location:	Korea, Taiwan
F. Date of Initial Production:	July 21, 2006

III. Packaging Information

A. Package Type:	100-pin TQFP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1240
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	21°C/W
M. Multi Layer Theta Jc:	2°C/W

IV. Die Information

A. Dimensions:	276X254 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{1000 \times 4340 \times 96 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 0.98 \times 10^{-9}$

$\lambda = 0.98$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.11 @ 25C and 1.87 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (ESD lot QSI1AQ003A D/C 0604, Latch-Up lot QSI0BQ001B D/C 0453)

The CA14-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1

Reliability Evaluation Test Results

MAX1436BECQ+D

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 1000 hrs.	DC Parameters & functionality	96	0	QSI0BQ002Q, D/C 0543

Note 1: Life Test Data may represent plastic DIP qualification lots.