RELIABILITY REPORT

FOR

MAX1421xCM

PLASTIC ENCAPSULATED DEVICES

April 6, 2004

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Manager, Reliability Operations

Reviewed by

Bryan J. Preeshl
Quality Assurance
Managing Director

Conclusion

The MAX1421 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1421 is a +3.3V, 12-bit analog-to-digital converter (ADC), featuring a fully-differential input, pipelined, 12-stage ADC architecture with wideband track-and-hold (T/H) and digital error correction incorporating a fully-differential signal path. The MAX1421 is optimized for low-power, high-dynamic performance applications in imaging and digital communications. The converter operates from a single +3.3V supply, consuming only 188mW while delivering a typical signal-to-noise ratio (SNR) of 66dB at an input frequency of 15MHz and a sampling frequency of 40Msps. The fully-differential input stage has a small signal -3dB bandwidth of 400MHz and may be operated with single-ended inputs.

An internal +2.048V precision bandgap reference sets the full-scale range of the ADC. A flexible reference structure accommodates an internal or externally applied buffered or unbuffered reference for applications requiring increased accuracy or a different input voltage range.

In addition to low operating power, the MAX1421 features two power-down modes, a reference power-down and a shutdown mode. In reference power-down, the internal bandgap reference is deactivated, resulting in a typical 2mA supply current reduction. For idle periods, a full shutdown mode is available to maximize power savings.

The MAX1421 provides parallel, offset binary, CMOS-compatible three-state outputs.

The MAX1421 is available in a 7mm x 7mm, 48-pin TQFP package, and is specified over the commercial (0°C to +70°C) and the extended industrial (-40°C to +85°C) temperature ranges.

Pin-compatible higher- and lower-speed versions of the MAX1421 are also available. Please refer to the MAX1420 data sheet for a frequency of 60Msps and the MAX1422 data sheet for a frequency of 20Msps.

B. Absolute Maximum Ratings

Item	Rating
AVDD, DVDD to AGND	-0.3V to +4V
DVDD, AVDD to DGND	-0.3V to +4V
DGND to AGND	-0.3V to +0.3V
INP, INN, REFP, REFN, REFIN, CML, CLK, CLK	(AGND - 0.3V) to (AVDD + 0.3V)
D0–D11, OE, PD	(DGND - 0.3V) to (DVDD + 0.3V)
Maximum Junction Temperature	+150°C
Operating Temperature Ranges	
MAX1421CCM	0°C to +70°C
MAX1421ECM	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
48-Pin TQFP	1000mW
Derates above +70°C	
48-Pin TQFP	12.5mW/°C

II. Manufacturing Information

A. Description/Function:	12-Bit, 40Msps, +3.3V, Low-Power ADC with Internal Reference
B. Process:	TC35 (.35 Micron CMOS)
C. Number of Device Transistors:	7310
D. Fabrication Location:	Taiwan
E. Assembly Location:	Korea or Malaysia
F. Date of Initial Production:	July, 2001

III. Packaging Information

A. Package Type:	**48-Pin TQFP**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-2101-0025
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-A:	Level 1

IV. Die Information

A. Dimensions:	117 x 106 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal 1 = 0.5 / Metal 2 = 0.6 / Metal 3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal 1 = 0.45 / Metal 2 = 0.5 / Metal 3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 160 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 6.79 \times 10^{-9}$

$\lambda = 6.79$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5595) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The AC07 die type has been found to have all pins able to withstand a transient pulse of ±1000V Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX1421ECM

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		160	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TQFP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

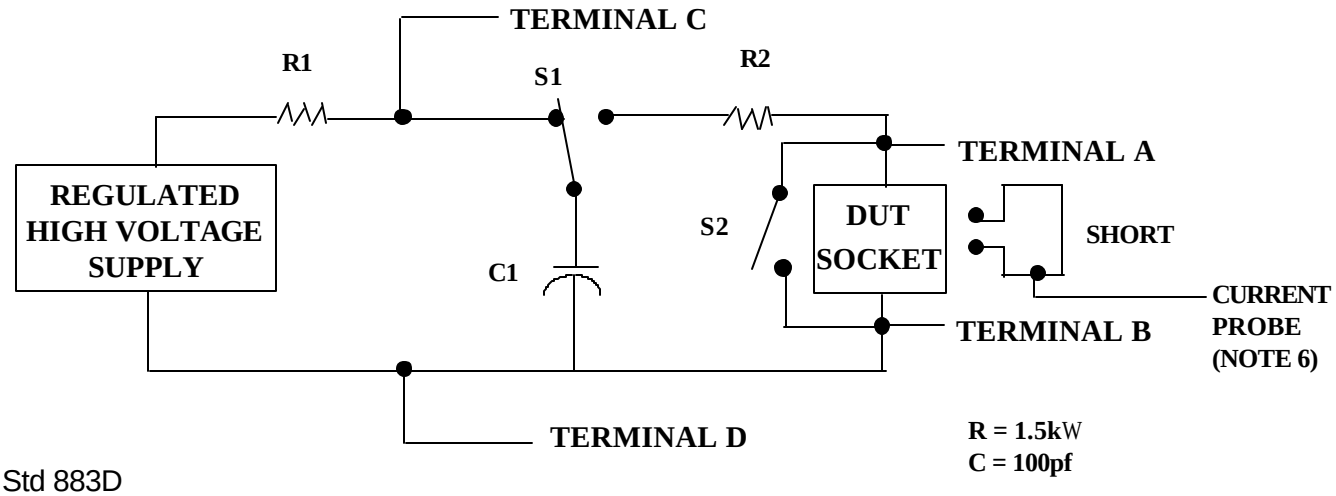
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

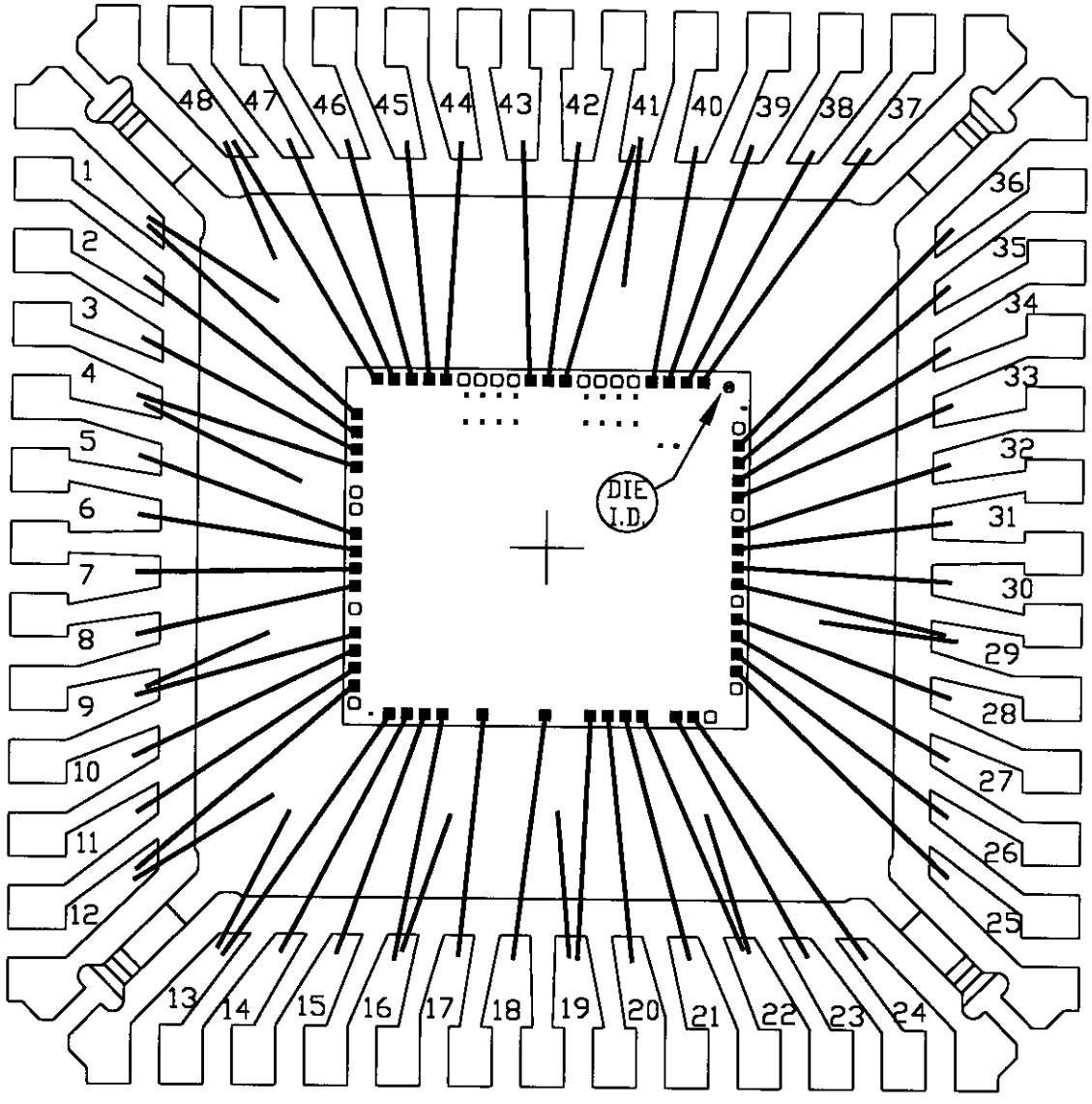
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

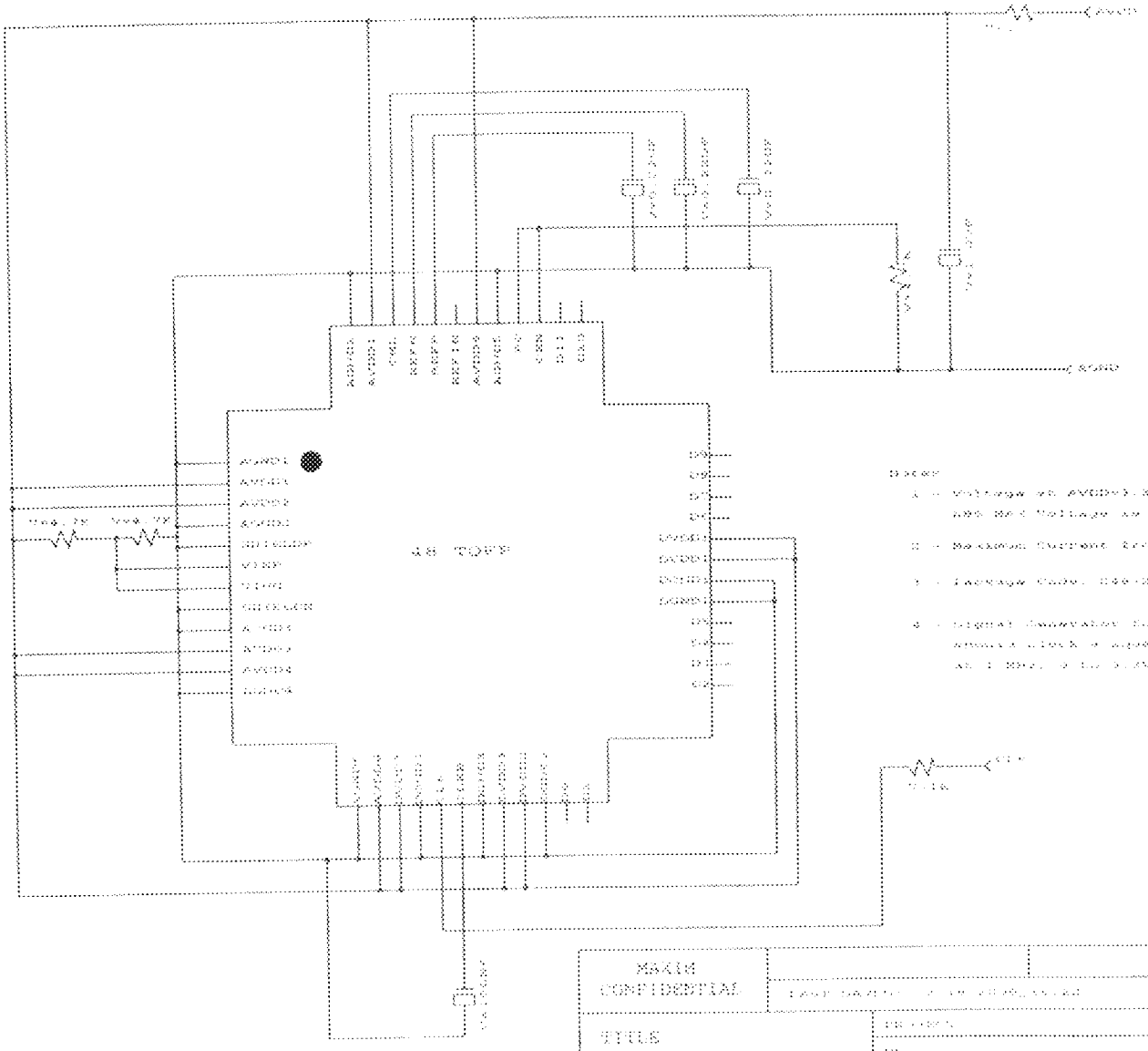


Mil Std 883D
Method 3015.7
Notice 8



PKG. CODE: C48-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 190X190	PKG. DESIGN			BOND DIAGRAM #: 05-2101-0025	REV: A

DEVICES
MAX1420
MAX1421
MAX1422
MAX1423



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