RELIABILITY REPORT

FOR

MAX1294BCEI+T

PLASTIC ENCAPSULATED DEVICES

February 13, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX1294BCEI+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1294/MAX1296 low-power, 12-bit analog-to-digital converters (ADCs) feature a successive-approximation ADC, automatic power-down, fast wake-up (2µs), an on-chip clock, +2.5V internal reference, and a high-speed 12-bit parallel interface. They operate with a single +5V analog supply. Power consumption is only 10mW at the maximum sampling rate of 420ksps. Two software-selectable power-down modes enable the MAX1294/MAX1296 to be shut down between conversions; accessing the parallel interface returns them to normal operation. Powering down between conversions can reduce supply below 10µA at lower sampling rates. Both devices offer software-configurable analog inputs for unipolar/bipolar and single-ended/pseudo-differential operation. In single-ended mode, the MAX1294 has six input channels and the MAX1296 has two (three input channels and one input channel, respectively, when in pseudo-differential mode). Excellent dynamic performance and low power, combined with ease of use and small package size, make these converters ideal for battery-powered and data-acquisition applications or for other circuits with demanding power-consumption and space requirements. The MAX1294/MAX1296 tri-states active-low INT when active-low CS goes high. Refer to MAX1266/MAX1268 if tri-stating active-low INT is not desired. The MAX1294 is offered in a 28-pin QSOP package, while the MAX1296 is available in a 24-pin QSOP. For pin-compatible +3V, 12-bit versions, see the MAX1295/MAX1297.

II. Manufacturing Information

A. Description/Function:	420ksps, +5V, 6-/2-Channel, 12-Bit ADCs with +2.5V Reference and Parallel Interface
B. Process:	B12
C. Number of Device Transistors:	5761
D. Fabrication Location:	Oregon, California or Texas
E. Assembly Location:	Malaysia, Philippines, Thailand
F. Date of Initial Production:	October 23, 1999

III. Packaging Information

A. Package Type:	28-pin QSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-0101-0495
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	93°C/W
K. Single Layer Theta Jc:	27°C/W
L. Multi Layer Theta Ja:	79.3°C/W
M. Multi Layer Theta Jc:	27°C/W

IV. Die Information

A. Dimensions:	86 X 160 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135¿C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 130 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 8.4 \times 10^{-9}$

$\lambda = 8.4$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the B12 Process results in a FIT Rate of 0.06 @ 25C and 1.06 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot I9EAD2018D D/C 0118)

The AD92 die type has been found to have all pins able to withstand a HBM transient pulse of +/1000V Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1

Reliability Evaluation Test Results

MAX1294BCEI+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	80	0	I9EADA019J, D/C 0214
	Biased	& functionality	50	0	J9EAFQ002H, D/C 0826
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.