MAX1291xxEI Rev. A

RELIABILITY REPORT

FOR

MAX1291xxEI

PLASTIC ENCAPSULATED DEVICES

February 14, 2003

MAXIM INTEGRATED PRODUCTS

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Written by

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Conclusion

The MAX1291 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1291 low-power, 12-bit analog-to-digital converter (ADC) features a successive-approximation ADC, automatic power-down, fast wake-up (2 μ s), an on-chip clock, +2.5V internal reference, and a high-speed, byte-wide parallel interface. It operates with a single +3V analog supply and feature a V_{LOGIC} pin that allows it to interface directly with a +1.8V to +5.5V digital supply.

Power consumption is only 5.7mW ($V_{DD} = V_{LOGIC}$) at the maximum sampling rate of 250ksps. Two software-selectable powerdown modes enable the MAX1291/ MAX1293 to be shut down between conversions; accessing the parallel interface returns them to normal operation. Powering down between conversions can cut supply current to under 10µA at reduced sampling rates.

The devices offers software-configurable analog inputs for unipolar/bipolar and single-ended/pseudo-differential operation. In single-ended mode, the MAX1291 has eight input channels.

Excellent dynamic performance and low power combined with ease of use and small package size make this converter ideal for battery-powered and data-acquisition applications or for other circuits with demanding power consumption and space requirements.

The MAX1291 is available in a 28-pin QSOP package.

B. Absolute Maximum Ratings Item	Rating
VDD to GND	-0.3V to +6V
VLOGIC to GND	-0.3V to +6V
CH0–CH7, COM to GND	-0.3V to (VDD + 0.3V)
REF, REFADJ to GND	-0.3V to (VDD + 0.3V)
Digital Inputs to GND	-0.3V to +6V
Digital Outputs (D0–D11, INT) to GND	-0.3V to (VLOGIC + 0.3V)
Operating Temperature Ranges MAX1291_C_ MAX1291_E_ Storage Temperature Range Lead Temperature (soldering, 10s) Continuous Power Dissipation (TA = +70°C) 28-Pin QSOP Derates above +70°C 28-Pin QSOP	0°C to +70°C -40°C to +85°C -65°C to +150°C +300°C 667mW 8.0mW/°C

II. Manufacturing Information

A. Description/Function: 250ksps, +3V, 8-/4-Channel, 12-Bit ADCs with +2.5V Reference and Parallel Interface

B. Process:	S12 (Standard 1.2 micron silicon gate CMOS)
C. Number of Device Transistors:	5781
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia, Thailand or Philippines
F. Date of Initial Production:	October, 1999

III. Packaging Information

A. Package Type:	28-Pin QSOP
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05- 0101-0490
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity	

per JEDEC standard JESD22-112: Level 1

IV. Die Information

A. Dimensions:	86 x 160 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

Α.	Quality Assurance Contacts:	Jim Pedicord (Reliability Lab Manager)
		Bryan Preeshl (Executive Director)
		Kenneth Huening (Vice President)

- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°Cbiased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

 $\lambda = \underbrace{1}_{\text{MTTF}} = \underbrace{\frac{1.83}{192 \times 4389 \times 240 \times 2}}_{\text{Temperature Acceleration factor assuming an activation energy of 0.8eV}$ $\lambda = 4.52 \times 10^{-9}$

 $h = 4.52 \times 10$

 λ = 4.52 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5426) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The AD92 die type has been found to have all pins able to withstand a transient pulse of $\pm 1000V$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ± 250 mA.

Table 1 Reliability Evaluation Test Results

MAX1291xxEI

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	: (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		240	0
Moisture Testir	ng (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Str	ess (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots. Note 2: Generic Package/Process data

Attachment #1

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

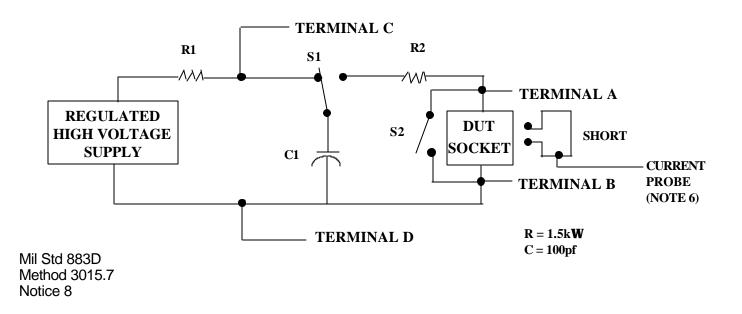
TABLE II. Pin combination to be tested. 1/2/

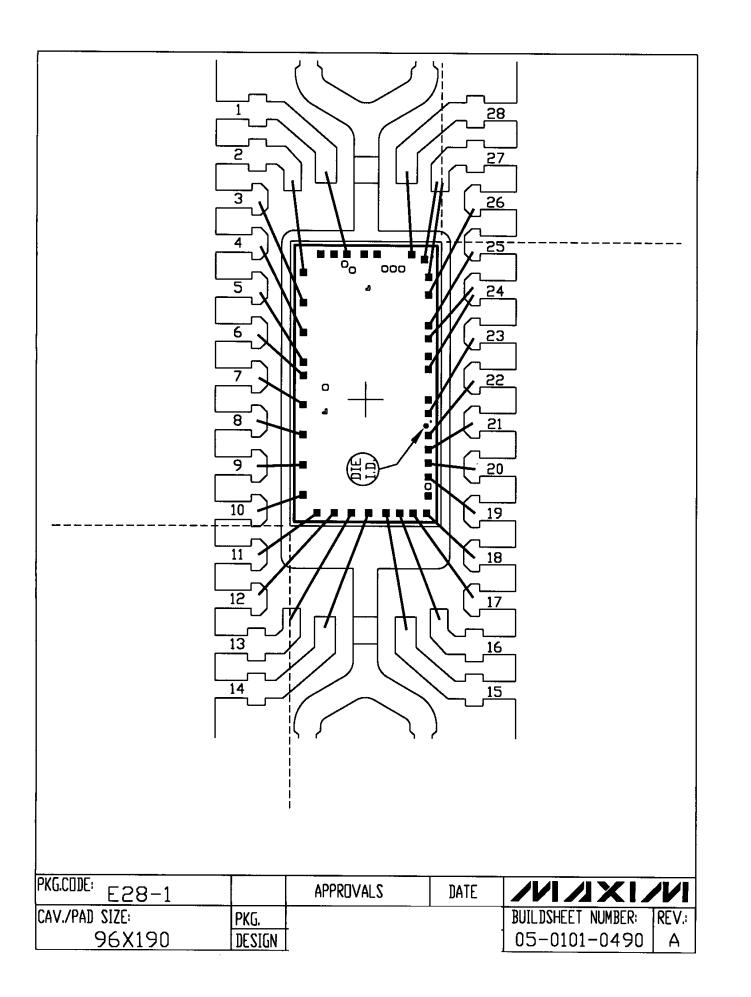
- 1/ Table II is restated in narrative form in 3.4 below.
- $\overline{2/}$ No connects are not to be tested.
- $\overline{3/}$ Repeat pin combination I for each named Power supply and for ground

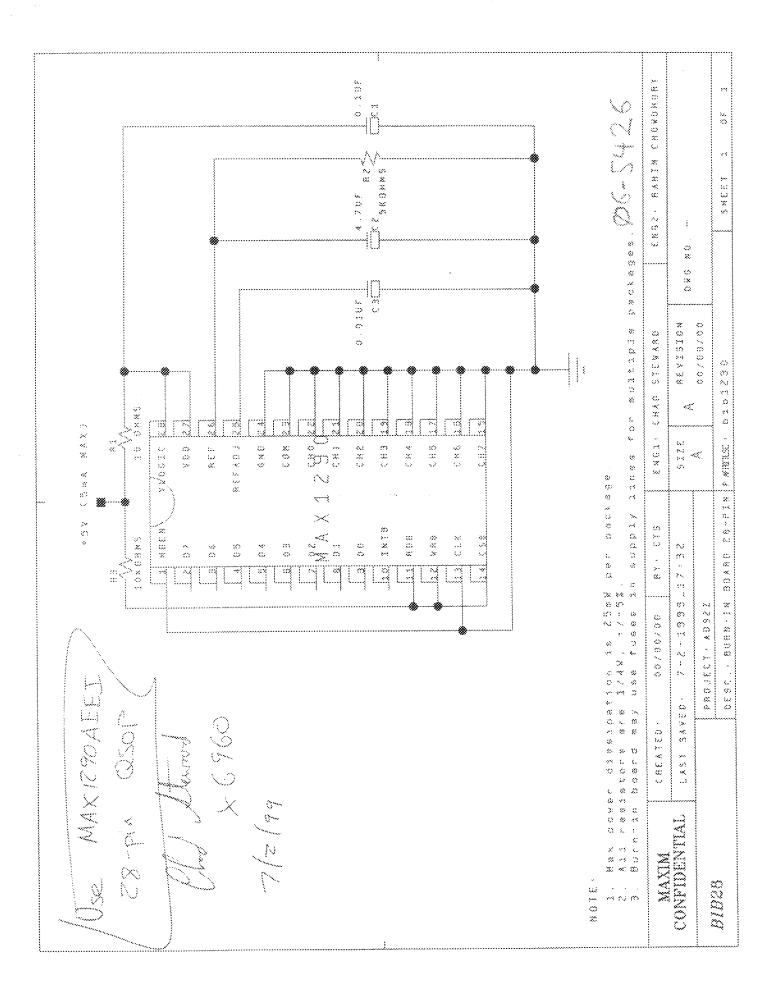
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, + V_{S} , - V_{S} , V_{REF} , etc).

3.4 <u>Pin combinations to be tested.</u>

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.







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