RELIABILITY REPORT

FOR

MAX12557ETK+

PLASTIC ENCAPSULATED DEVICES

February 8, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX12557ETK+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX12557 is a dual 3.3V, 14-bit analog-to-digital converter (ADC) featuring fully differential wideband track-and-hold (T/H) inputs, driving internal quantizers. The MAX12557 is optimized for low power, small size, and high dynamic performance in intermediate frequency (IF) and baseband sampling applications. This dual ADC operates from a single 3.3V supply, consuming only 610mW while delivering a typical 72.5dB signal-to-noise ratio (SNR) performance at a 175MHz input frequency. The T/H input stages accept single-ended or differential inputs up to 400MHz. In addition to low operating power, the MAX12557 features a 166µW powerdown mode to conserve power during idle periods. A flexible reference structure allows the MAX12557 to use the internal 2.048V bandgap reference or accept an externally applied reference and allows the reference to be shared between the two ADCs. The reference structure allows the full-scale analog input range to be adjusted from ±0.35V to ±1.15V. The MAX12557 provides a common-mode reference to simplify design and reduce external component count in differential analog input circuits. The MAX12557 supports either a single-ended or differential input clock. User-selectable divide-by-two (DIV2) and divide-by-four (DIV4) modes allow for design flexibility and help eliminate the negative effects of clock jitter. Wide variations in the clock duty cycle are compensated with the ADC's internal duty-cycle equalizer (DCE). The MAX12557 features two parallel, 14-bit-wide, CMOS-compatible outputs. The digital output format is pin-selectable to be either two's complement or Gray code. A separate power-supply input for the digital outputs accepts a 1.7V to 3.6V voltage for flexible interfacing with various logic levels. The MAX12557 is available in a 10mm x 10mm x 0.8mm, 68-pin thin QFN package with exposed paddle (EP), and is specified for the extended (-40°C to +85°C) temperature range.

II. Manufacturing Information

A. Description/Function:	Dual, 65Msps, 14-Bit, IF/Baseband ADC
B. Process:	TS18
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	China, Thailand
F. Date of Initial Production:	January 21, 2005

III. Packaging Information

A. Package Type:	68-pin TQFN 10x10
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2288
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	34°C/W
K. Single Layer Theta Jc:	0.4°C/W
L. Multi Layer Theta Ja:	20°C/W
M. Multi Layer Theta Jc:	0.4°C/W

IV. Die Information

A. Dimensions:	173 X 204 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18µm
F. Minimum Metal Spacing:	0.18µm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 192 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 5.60 \times 10^{-9}$

$\lambda = 5.60$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.24 @ 25C and 4.14 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The CA16-2 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000 V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1

Reliability Evaluation Test Results

MAX12557ETK+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	192	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data