RELIABILITY REPORT

FOR

MAX12528ETK+

PLASTIC ENCAPSULATED DEVICES

November 22, 2011

MAXIM INTEGRATED PRODUCTS

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Approved by
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Quality Assurance
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Conclusion

The MAX12528ETK+D successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX12528 is a dual 80Msps, 12-bit analog-to-digital converter (ADC) featuring fully differential wideband track-and-hold (T/H) inputs, driving internal quantizers. The MAX12528 is optimized for low power, small size, and high dynamic performance in intermediate frequency (IF) and baseband sampling applications. This dual ADC operates from a single 3.3V supply, consuming only 726mW while delivering a typical 69.8dB signal-tonoise ratio (SNR) performance at a 175MHz input frequency. The T/H input stages accept single-ended or differential inputs up to 400MHz. In addition to low operating power, the MAX12528 features a 330µW powerdown mode to conserve power during idle periods. A flexible reference structure allows the MAX12528 to use the internal 2.048V bandgap reference or accept an externally applied reference and allows the reference to be shared between the two ADCs. The reference structure allows the full-scale analog input range to be adjusted from ±0.35V to ±1.15V. The MAX12528 provides a common-mode reference to simplify design and reduce external component count in differential analog input circuits. The MAX12528 supports either a single-ended or differential input clock. User-selectable divide-by-two (DIV2) and divide-by-four (DIV4) modes allow for design flexibility and help eliminate the negative effects of clock jitter. Wide variations in the clock duty cycle are compensated with the ADC's internal duty-cycle equalizer (DCE). The MAX12528 features two parallel, 12-bit-wide, CMOS-compatible outputs. The digital output format is pin-selectable to be either two's complement or Gray code. A separate power-supply input for the digital outputs accepts a 1.7V to 3.6V voltage for flexible interfacing with various logic levels. The MAX12528 is available in a 10mm x 10mm x 0.8mm, 68-pin thin QFN package with exposed paddle (EP), and is specified for the extended (-40°C to +85°C) temperature range. See a parametric table of the complete family of pin-compatible, 12-/14-bit high-speed ADCs.

II. Manufacturing Information

A. Description/Function:	Dual, 80Msps, 12-Bit, IF/Baseband ADC
B. Process:	TS18
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Thailand
F. Date of Initial Production:	April 20, 2005

III. Packaging Information

A. Package Type:	68L TQFN 10x10
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2289 / A
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	3
J. Single Layer Theta Ja:	34°C/W
K. Single Layer Theta Jc:	0.5°C/W
L. Multi Layer Theta Ja:	20°C/W
M. Multi Layer Theta Jc:	0.5°C/W

IV. Die Information

A. Dimensions:	173 X 204 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18µm
F. Minimum Metal Spacing:	0.18µm
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 144 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 7.6 \times 10^{-9}$

$\lambda = 7.6$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.24 @ 25C and 4.14 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (ESD lot QSU2BA004E D/C 0608, Latch-Up lot QSU2AQ002G D/C 0508)

The CA16-2 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX12528ETK+D

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	48	0	QSU4BQ001C, D/C 0621
	Biased	& functionality	48	0	QSU3AQ001E, D/C 0535
	Time = 192 hrs.		48	0	QSU2AQ002D, D/C 0449

Note 1: Life Test Data may represent plastic DIP qualification lots.