

RELIABILITY REPORT

FOR

MAX1232CPA+/MAX1232ESA+/MAX1232CSA+

PLASTIC ENCAPSULATED DEVICES

December 19, 2008

# **MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR. SUNNYVALE, CA 94086

Approved by	
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Quality Assurance	
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#### Conclusion

The MAX1232CPA+/MAX1232ESA+/MAX1232CSA+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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#### I. Device Description

#### A. General

The MAX1232 microprocessor ( $\mu$ P) supervisory circuit provides  $\mu$ P housekeeping and power-supply supervision functions while consuming only 1/10th the power of the DS1232. The MAX1232 enhances circuit reliability in  $\mu$ P systems by monitoring the power supply, monitoring the software execution, and providing a debounced manual reset input. The MAX1232 is a plug-in upgrade of the Dallas DS1232. A reset pulse of at least 250ms duration is supplied on power-up, power-down, and low-voltage brownout conditions (5% or 10% supply tolerances can be selected digitally). Also featured is a debounced manual reset input that forces the reset outputs to their active states for a minimum of 250ms. A digitally programmable watchdog timer monitors software execution and can be programmed for timeout settings of 150ms, 600ms, or 1.2s. The MAX1232 requires no external components.



### II. Manufacturing Information

A. Description/Function: Microprocessor Monitor

B. Process: MFN Standard Metal Gate CMOS (M6)

C. Number of Device Transistors:

D. Fabrication Location: Oregon

E. Assembly Location: Thailand, Philippines, Malaysia

F. Date of Initial Production: Pre 1997

#### III. Packaging Information

A. Package Type: 8-pin PDIP/ 8-pin SOIC

B. Lead Frame: Copper

C. Lead Finish:

D. Die Attach:

Conductive Epoxy

E. Bondwire:

Gold (1.3 mil dia.)

F. Mold Material:

G. Assembly Diagram:

#05-0701-0363

H. Flammability Rating:

Class UL94-V0

I. Classification of Moisture Sensitivity per Level 1

JEDEC standard J-STD-020-C

J. Single Layer Theta Ja: 110°C/WK. Single Layer Theta Jc: 40°C/W

#### IV. Die Information

A. Dimensions: 70 X 103 mils

B. Passivation: Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub> (Silicon nitride/ Silicon dioxide

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
 F. Minimum Metal Spacing: Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.
 H. Isolation Dielectric: SiO<sub>2</sub>
 I. Die Separation Method: Wafer Saw



#### V. Quality Assurance Information

A. Quality Assurance Contacts: Ken Wendel (Director, Reliability Engineering)

Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm</li>D. Sampling Plan: Mil-Std-105D

#### VI. Reliability Evaluation

#### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\frac{\lambda = \frac{1}{\text{MTTF}}}{= \frac{1.83}{192 \times 4340 \times 640 \times 2}}$$
 (Chi square value for MTTF upper limit) (where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$x = 1.7 \times 10^{-9}$$

A = 1.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maximic.com/. Current monitor data for the M6 Process results in a FIT Rate of 3.2 @ 25C and 54.8 @ 55C (0.8 eV, 60% UCL)

#### B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

## C. E.S.D. and Latch-Up Testing

The PS68 die type has been found to have all pins able to withstand a HBM transient pulse of +/-3000 V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250 mA.



# Table 1

## Reliability Evaluation Test Results

## MAX1232CPA+/MAX1232ESA+/MAX1232CSA+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	
Static Life Test (	(Note 1)				
	Ta = 135°C	DC Parameters	640	0	
	Biased Time = 192 hrs.	& functionality			
Moisture Testing	(Note 2)				
85/85	Ta = 85°C	DC Parameters	77	0	
	RH = 85%	& functionality			
	Biased				
	Time = 1000hrs.				
Mechanical Stres	ss (Note 2)				
Temperature	-65°C/150°C	DC Parameters	77	0	
Cycle	1000 Cycles	& functionality			
	Method 1010				

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data