RELIABILITY REPORT

FOR

MAX1230xxxx

PLASTIC ENCAPSULATED DEVICES

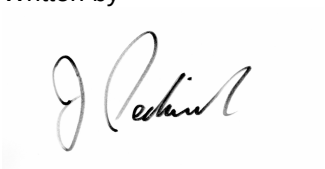
October 18th, 2004

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by

Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX1230 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1230 is a serial 12-bit analog-to-digital converters (ADCs) with an internal reference and an internal temperature sensor. This device features on-chip FIFO, scan mode, internal clock mode, internal averaging, and AutoShutdown™. The maximum sampling rate is 300ksps using an external clock. The MAX1230 has 16 input channels. All input channels are configurable for single-ended or differential inputs in unipolar or bipolar mode. The device operates from a +5V supply and contain a 10MHz SPI™/QSPI™/MICROWIRE™-compatible serial port.

The MAX1230 is available in 28-pin 5mm x 5mm QFN with exposed pad and 24-pin QSOP packages. The device is specified over the extended -40°C to +85°C temperature range.

B. Absolute Maximum Ratings

Item	Rating
VDD to GND	-0.3V to +6V
CS, SCLK, DIN, EOC, DOUT to GND	-0.3V to (VDD + 0.3V)
AIN0–AIN13, REF-/AIN_, CNVST/AIN_, REF+ to GND	-0.3V to (VDD + 0.3V)
Maximum Current into Any Pin	50mA
Operating Temperature Ranges	
MAX1030C__	0°C to +70°C
MAX1030E__	-40°C to +85°C
Storage Temperature Range	-60°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
24-Pin QSOP	762mW
28-Pin QFN (5mm x 5mm)	1667mW
Derates above +70°C	
24-Pin QSOP	9.5mW/°C
28-Pin QFN (5mm x 5mm)	20.8mW/°C

II. Manufacturing Information

A. Description/Function:	12-Bit 300ksps ADCs with FIFO, Temp Sensor, Internal Reference
B. Process:	S6 BiCMOS process
C. Number of Device Transistors:	30,889
D. Fabrication Location:	California, USA
E. Assembly Location:	Malaysia, Philippines, Hong Kong or Thailand
F. Date of Initial Production:	April, 2003

III. Packaging Information

A. Package Type:	**24-Lead QSOP**	**28-Lead QFN (5x5)**
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-Filled Epoxy	Silver-Filled Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-9000-0241	Buildhseet #05-9000-0242
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	86 x 120 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	TiW/ AlCu/ TiWN
D. Backside Metallization:	None
E. Minimum Metal Width:	.6 microns (as drawn)
F. Minimum Metal Spacing:	.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 47 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 23.10 \times 10^{-9}$ $\lambda = 23.10$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-6080) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**) located on the Maxim website at http://www.maxim-ic.com .

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AC19 die type has been found to have all pins able to withstand a transient pulse of ±1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX1230xxxx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	47	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

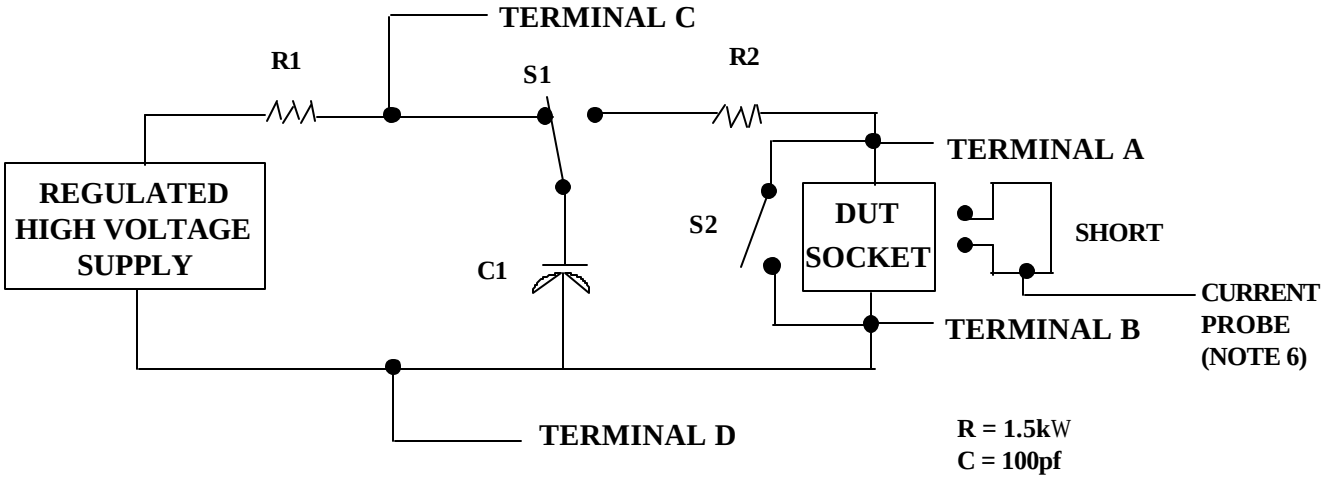
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

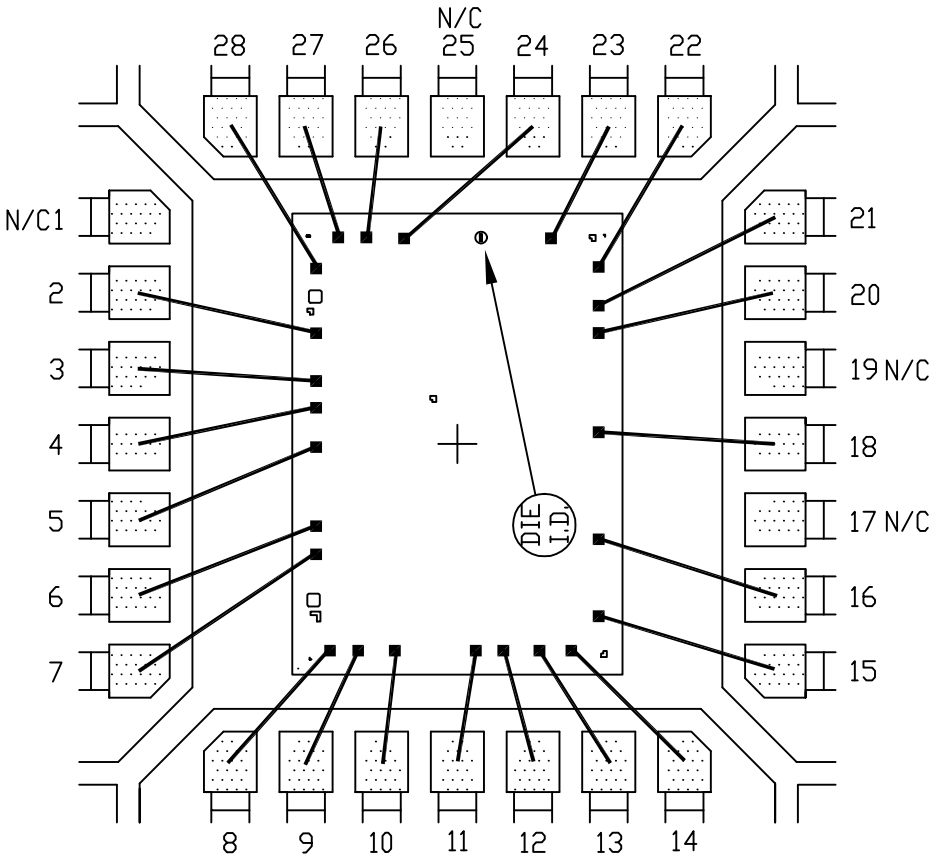
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

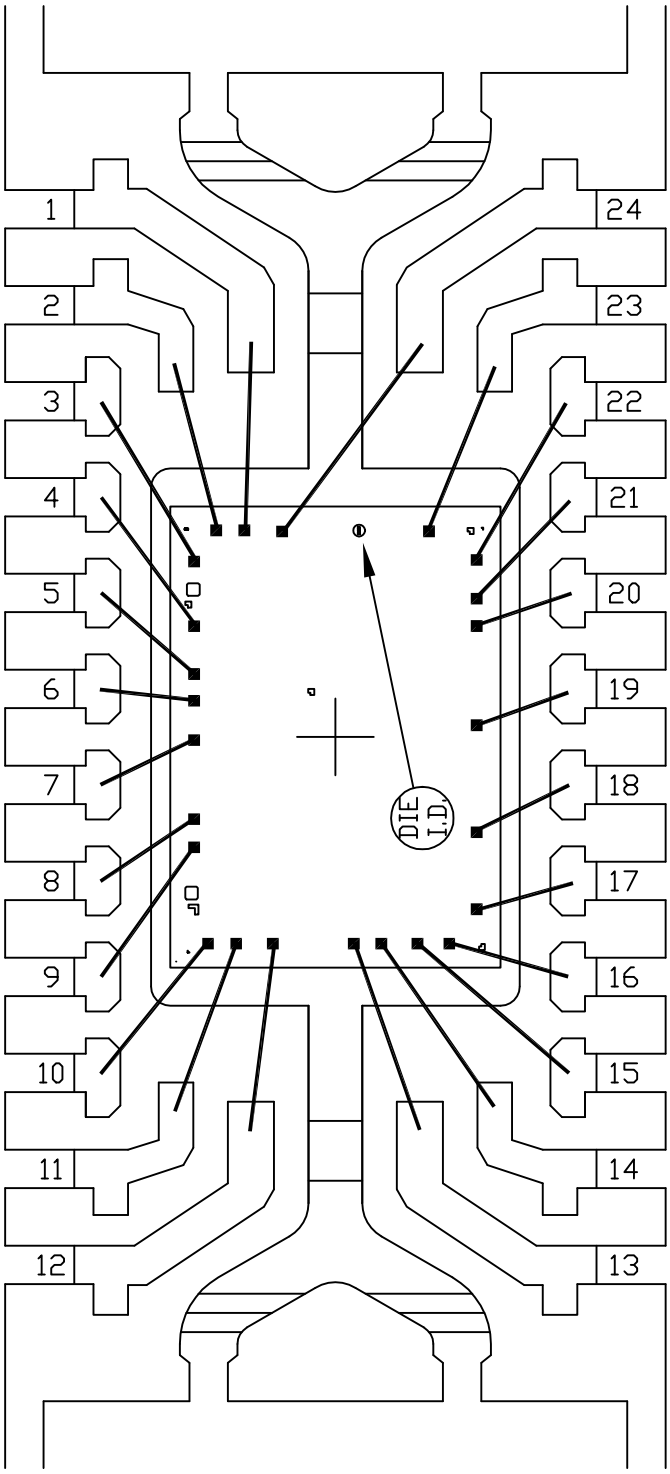


5x5x0.8mm THIN QFN PKG. EXPOSED PAD PKG.



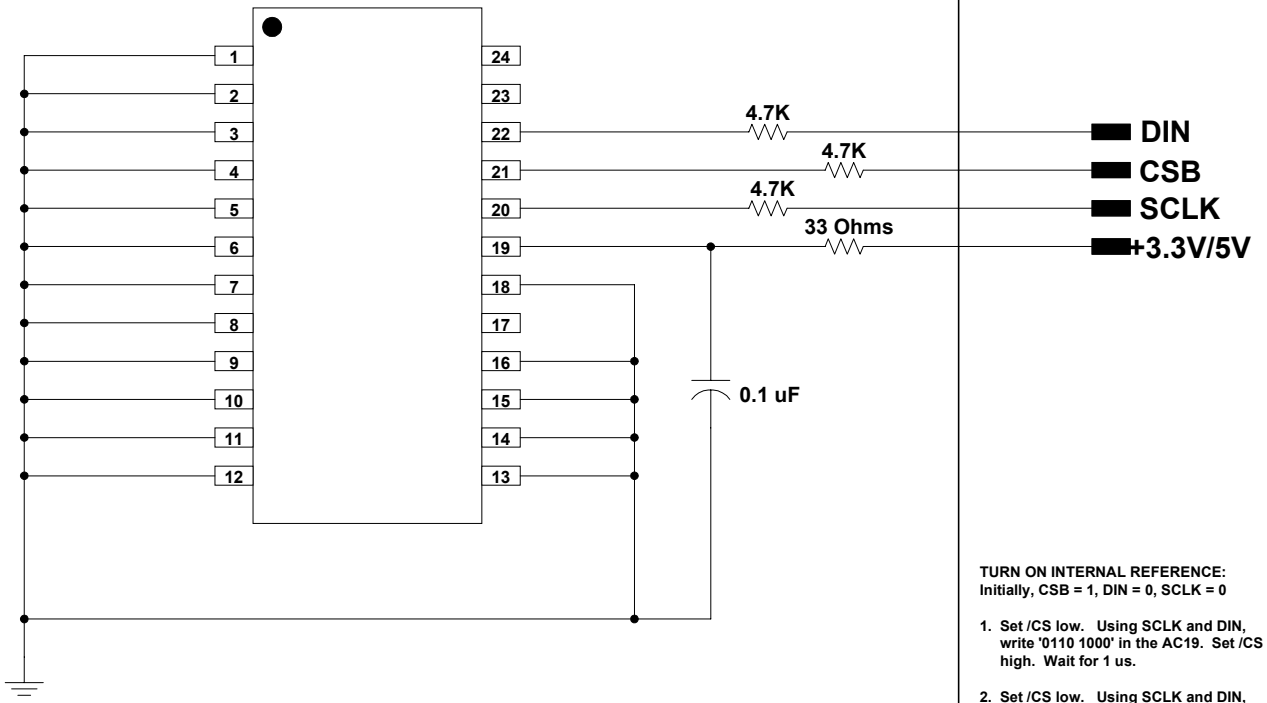
BONDABLE AREA

PKG. CODE: T2855-6		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 138x138	PKG.			BOND DIAGRAM #: 05-9000-0242	REV: B
	DESIGN				



PKG. CODE: E24-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 96X140	PKG.			BOND DIAGRAM #: 05-9000-0241	REV: A
	DESIGN				

ONCE PER SOCKET



ONCE PER BOARD

TURN ON INTERNAL REFERENCE:
Initially, CSB = 1, DIN = 0, SCLK = 0

1. Set /CS low. Using SCLK and DIN, write '0110 1000' in the AC19. Set /CS high. Wait for 1 us.
2. Set /CS low. Using SCLK and DIN, write '1000 0110' into the AC19. Set /CS high. Wait for 1 us.
3. Wait for 150 us.

DEVICES: MAX 1230/1231
PACKAGE: 24-QSOP
MAX. EXPECTED CURRENT = 1.5mA (+3V) OR (+5V)

DRAWN BY: TEK TAN
NOTES: +3.3V FOR MAX1031/1231.
+5V FOR MAX1030/1230.

SPI Input Timing

Applies to MAX1230,1231,1030, and 1031

Vih= VDD

Vil= 0V

SCLK Frequency= 200 Khz