RELIABILITY REPORT

FOR

MAX1213NEGK+

PLASTIC ENCAPSULATED DEVICES

December 3, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX1213NEGK+D successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX1213N is a monolithic, 12-bit, 170Msps analog-to-digital converter (ADC) optimized for outstanding dynamic performance at high-IF frequencies beyond 300MHz. The product operates with conversion rates up to 170Msps while consuming only 720mW. At 170Msps and an input frequency up to 100MHz, the MAX1213N achieves an 87dBc spurious-free dynamic range (SFDR) with excellent 67.2dB signal-to-noise ratio (SNR) that remains flat (within 2dB) for input tones up to 250MHz. This makes it ideal for wideband applications such as communications receivers, cable-head end receivers, and power-amplifier predistortion in cellular base-station transceivers. The MAX1213N operates from a single 1.8V power supply. The analog input is designed for AC-coupled differential or single-ended operation. The ADC also features a selectable on-chip divide-by-2 clock circuit that accepts clock frequencies as high as 340MHz. A low-voltage differential signal (LVDS) sampling clock is recommended for best performance. The converter provides LVDS-compatible digital outputs with data format selectable to be either two's complement or offset binary. The MAX1213N is available in a 68-pin QFN package with exposed paddle (EP) and is specified over the industrial (-40°C to +85°C) temperature range. See a parametric table of the complete family of pin-compatible, 8-/10-/12-bit high-speed ADCs.

II. Manufacturing Information

A. Description/Function:	1.8V, Low-Power, 12-Bit, 170Msps ADC for Broadband Applications
B. Process:	TS18
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Korea
F. Date of Initial Production:	April 21, 2006

III. Packaging Information

A. Package Type:	68-pin QFN 10x10
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0843
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	35°C/W
K. Single Layer Theta Jc:	0.8°C/W
L. Multi Layer Theta Ja:	24°C/W
M. Multi Layer Theta Jc:	0.8°C/W

IV. Die Information

A. Dimensions:	185 X 141 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18µm
F. Minimum Metal Spacing:	0.18µm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 141 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 7.62 \times 10^{-9}$

λ = 7.62 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.24 @ 25C and 4.14 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The CA07-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500 V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1

Reliability Evaluation Test Results

MAX1213NEGK+D

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	141	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data