

RELIABILITY REPORT

FOR

MAX11905ETP+

PLASTIC ENCAPSULATED DEVICES

December 18, 2015

MAXIM INTEGRATED

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Approved by		
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Quality Assurance		
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Conclusion

The MAX11905ETP+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX11905 is a 20-bit, 1.6Msps, single-channel, fully differential SAR ADC with internal reference buffers. The MAX11905 provides excellent static and dynamic performance with best-in-class power consumption that directly scales with throughput. The device has a unipolar differential ±V REF input range. Supplies include a 3.3V supply for the reference buffers, a 1.8V analog supply, a 1.8V digital supply, and a 1.5V to 3.6V digital interface supply. This ADC achieves 98.3dB SNR and -123dB THD, guarantees 20-bit resolution with no-missing codes and 6 LSB INL (max). The MAX11905 communicates data using a SPI-compatible serial interface. The MAX11905 is offered in a 20-pin, 4mm x 4mm, TQFN package and is specified over the -40°C to +85°C operating temperature range.



II. Manufacturing Information

A. Description/Function: 20-Bit, 1.6Msps, Low-Power, Fully Differential SAR ADC

B. Process: TS18
C. Number of Device Transistors: 201572
D. Fabrication Location: Taiwan
E. Assembly Location: Taiwan

F. Date of Initial Production: February 14, 2014

III. Packaging Information

A. Package Type: 20L TQFN 4x4x0.75

B. Lead Frame: Copper

C. Lead Finish: 100% matte Tin
D. Die Attach: Conductive
E. Bondwire: Au (1 mil dia.)
F. Mold Material: Epoxy with silica filler
G. Assembly Diagram: #05-9000-5308
H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per

JEDEC standard J-STD-020-C

J. Single Layer Theta Ja: 48°C/W
K. Single Layer Theta Jc: 2°C/W
L. Multi Layer Theta Ja: 33°C/W
M. Multi Layer Theta Jc: 2°C/W

IV. Die Information

A. Dimensions: 100X100 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Al/0.5%Cu with Ti/TiN Barrier

D. Backside Metallization: NoneE. Minimum Metal Width: 0.18umF. Minimum Metal Spacing: 0.18um

G. Bondpad Dimensions:

H. Isolation Dielectric: SiO₂I. Die Separation Method: Wafer Saw



V. Quality Assurance Information

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)

Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppmD. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (1) is calculated as follows:

$$x = 13.9 \times 10^{-9}$$

 $x = 13.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.11 @ 25C and 1.87 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot QAOL6A029C, D/C 1335)

The AC90-0 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.



Table 1Reliability Evaluation Test Results

MAX11905ETP+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (No	ote 1) Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	79	0	QAOL6A029C, D/C 1335

Note 1: Life Test Data may represent plastic DIP qualification lots.